MITEL
SEMICONDUCTOR

GP2021

GPS 12 channel Correlator

Advance Information

DS4077 - 2.6 July 1996

The GP2021 is a 12 channel C/A code baseband correlator for use in NAVSTAR GPS and GLONASS satellite navigation receivers. The GP2021 complements the GP2015 and GP2010 C/A code RF downconverters available from Mitel Semiconductor.

The GP2021 is compatible with most 16 bit and 32 bit microprocessors, especially those from Motorola and Intel, with additional on–chip support for the ARM60 32 bit RISC processor. When the ARM60 is used, the on–chip memory management functions allow implementation of a full GPS receiver with minimal external logic.

The GP2021 allows individual channel de–activation, for systems not requiring full 12 channel operation, to save power and processor loading. Receiver power may be further conserved by reducing the supply voltage to 2.2V under battery backup. Although all system functions are disabled, the 32.768kHz oscillator and Real Time Clock are maintained for the microprocessor to estimate satellite visibility at power on to reduce signal acquisition time.

A development system called the GPS Architect is available as a basis for receiver design using the GP2021 and associated products.

FEATURES

- 12 Fully Independent Correlation Channels
- 1PPS UTC Aligned Timing Output
- On–Chip Dual UART and Real Time Clock
- Compatible with most 16 and 32 bit Microprocessors
- Memory Control Logic for ARM60 Microprocessor
- Low Voltage, Low Current Power–Down Mode
- Power Dissipation 150mW Typical
- Compatible with GP2015 and GP2010 RF Front Ends
- Battery Backup Voltage 2.2V (min)

APPLICATIONS

- GPS Navigation Systems
- High Integrity Combined GPS–GLONASS Receivers
- GPS Geodetic Receivers
- Time Transfer Receivers

ORDERING INFORMATION

GP2021/IG/GQ1R

RELATED PRODUCTS

PART	DESCRIPTION	DATASHEET REFERENCE
GP2015	GPS Receiver RF Front End – TQFP 48 package	DS4374
GP2010	GIPS Receiver RF Front End – PQFP 44 package	DS4056
DW9255	35.42MHz SAW Filter	DS3861
P60ARM	32 bit RISC Microprocessor	DS3553
GPS Architect	GPS 12 Channel Receiver Development System	DS4004

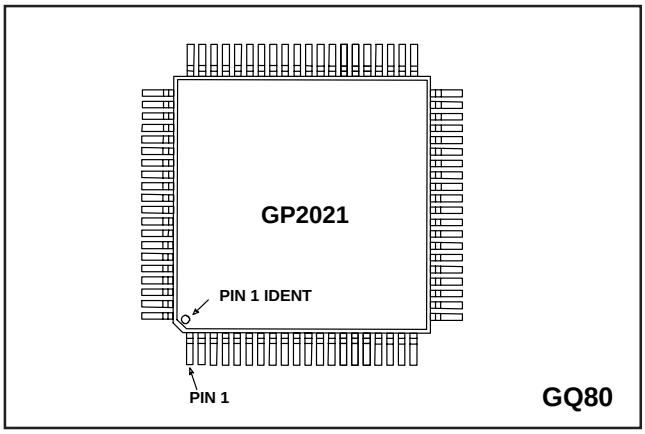

Fig.1 Pin connections - top view

PIN	DESCRIPTION	PIN	DESCRIPTION
1	MULTI_FN_IO	41	A6
2	POWER _GOOD	42	A5
3	NRESET_OP	43	A4
4	NARMSYS	44	A3
5	XIN	45	A2
6	XOUT	46	A1 / ALE_IP
7	TXA	47	A0 / NRESET_IP
8	TXB	48	D0
9	RXA	49	D1
10	RXB	50	D2
11	NROM / NC	51	D3
12	NEEPROM / NC	52	D4
13	NSPARE_CS / NC	53	D5
14	V_{DD}	54	D6
15	V_{SS}	55	V_{DD}
16	NRAM / BC	56	V_{SS}
17	NW0 / NC	57	D7
18	NW1 / NC	58	D8
19	NW2 / NC	59	D9
20	NW3 / NC	60	D10
21	NRD / NC	61	D11
22	ARM_ALE / NC	62	D12
23	DBE / NC	63	D13
24	ACCUM_INT	64	D14
25	MEAS_INT	65	D15
26	NBW / WRPROG	66	PLL_LOCK
27	NMREQ / DISCIP2	67	VDD
28	NOPC / NINTELMOT	68	DISCOP
29	NRW / DISCIP3	69	V_{SS}
30	MCLK / NC	70	CLK_T
31	ABORT / MICRO_CLK	71	CLK_I
32	DISCIO	72	V_{SS}
33	A22 / READ	73	SAMPCLK
34	VDD	74	V_{DD}
35	VSS	75	NBRAM / DISCIP4
36	A21 / NCS	76	SIGN0
37	A20 / WREN	77	MAG1
38	A9	78	SIGN1
39	A8	79	MAG1
40	A7	80	DISCIP1

TABLE OF CONTENTS

TYPICAL GPS RECEIVER

Fig. 2 shows a typical GPS receiver employing a GP2010 RF front–end, a GP2021 correlator and an ARM60 32 bit RISC microprocessor.

A single front end may be used, since all GPS satellites use the same L1 frequency of 1575.42 MHz. However, in order to achieve better sky coverage, it is sometimes desirable to use more than one antenna. In this case, separate front ends will be needed.

The RF section, GP2010, performs down conversion of the L1 signal for digital baseband processing. The resultant signal is then correlated in the GP2021 with an internally generated replica of the satellite code to be received. Individual codes for each channel may be selected independently to enable acquisition and tracking of up to 12 different satellites simultaneously

The results of the correlations form the accumulated data and are transferred to the microprocessor to give the broadcast satellite data (the 'Navigation Message') and to control the software signal tracking loops.

The GP2021 can be interfaced to one of two styles of front end. In Real_Input mode, the front end supplies either a 1 (sign) or 2 (sign and magnitude) bit signal to either the SIGN0/MAG0 or SIGN1/MAG1 inputs of the GP2021. Alteratively, in Real_Input mode, 2 separate front ends can be connected to a single GP2021 and selected under software control. The GP2015 and GP2010 are Real_Input mode front ends.

In Complex_Input mode, the front end is required to supply In–phase (I) and Quadrature (Q) signals to the SIGN0/MAG0 and SIGN1/MAG1 inputs respectively. Hence, only a single front end can be used with each GP2021 in Complex_Input mode.

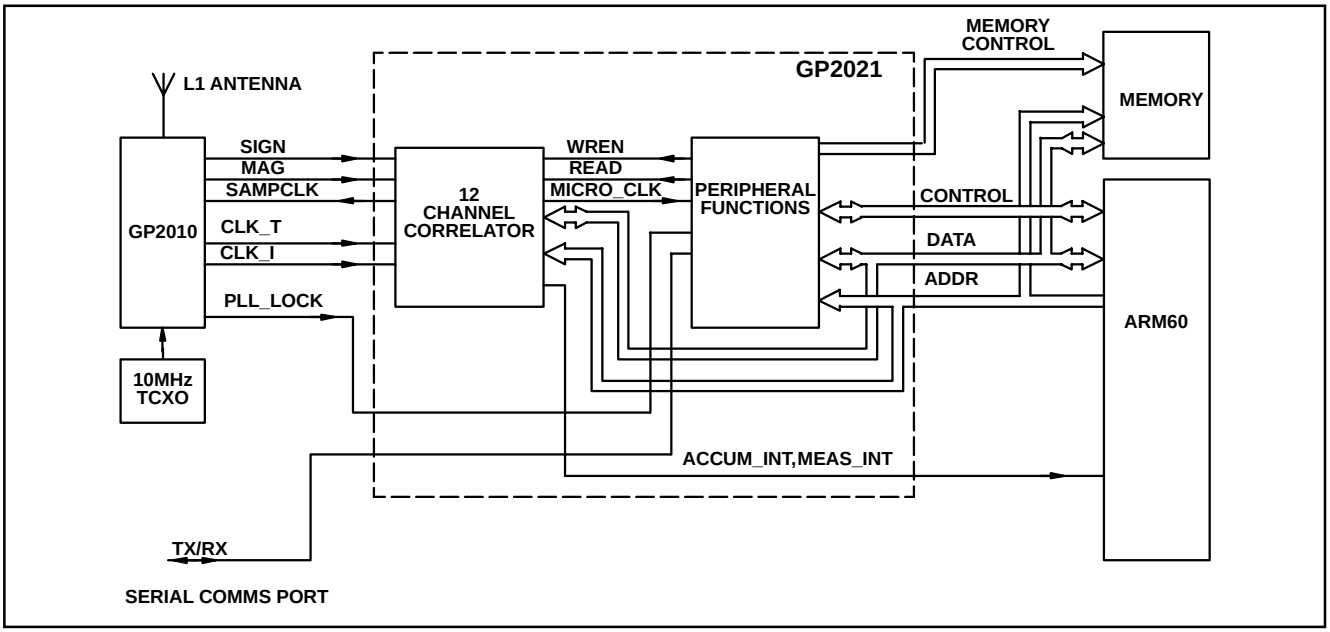

Fig. 2 Block diagram of typical ARM based receiver

PIN DESCRIPTION

All V SS and V DD pins must be connected in order to ensure reliable operation. Any unused inputs must be tied High or Low. The Table below describes the pin functions in Real_Input mode and assumes a master clock input frequency of 40MHz. Those pins whose functions differ in Complex_Input mode are described at the end of the table.

Note that those pin names containing a '/' have dual functionality between ARM System and Standard Interface modes. The Pin mnemonic for ARM System mode always precedes the '/'.

Pin No	Signal Name	Type	Description ARM System Mode	Description Standard Interface Mode
15, 35, 56, 69, 72	V SS	-	Ground Pin	
14, 34, 55, 67, 74	V DD	+	Power supply to device.	
1	MULTI_FN_IO	I/O	Multi–function input / output. Its function is configured by the IO_CONFIG register. After a GP2021 reset it acts as the Digital System Test Enable input. It can also be configured as a discrete output, or a discrete input if certain conditions are met.	
			Can be configured as the TRIGGER input to the DEBUG block in ARM System mode.	

Pin No	Signal Name	Type	Description ARM System Mode	Description Standard Interface Mode
2	POWER_GOOD	I	Power Monitor input. High for normal operation. Low forces the GP2021 into Power Down mode.	
3	NRESET_OP O		System Reset output (Active Low). Lasts for 4 MICRO_CLK cycles after all reset conditions have cleared.	
4	NARMSYS	I	Processor Mode Selection input. When Low, this input selects ARM System mode. When High, Standard Interface mode is selected.	
5	XIN	I	Crystal input connection to Real Time Clock.	
6	XOUT	O	Crystal output connection from Real Time Clock.	
7	TXA	O	Transmit Data output from Channel A of the Dual UART.	
8	TXB	O	Transmit Data output from Channel B of the Dual UART.	
9	RXA	1	Receive Data input to Channel A of the Dual UART. This pin acts as a master clock input in Digital System Test mode.	
10	RXB	I	Receive Data input to Channel B of the Dual UART. This pin acts as the Real Time Clock reset in Digital System Test mode.	
11	NROM / NC	O	ROM Chip Select output (Active Low).	Unused output. (Do not connect.)
12	NEEPROM / NC	O	EEPROM Chip Select output (Active Low)	Unused output. (Do not connect.)
13	NSPARE_CS / NC	O	Spare Chip Select output (Active Low).	Unused output. (Do not connect.)
16	NRAM / NC	O	RAM Chip Select output (Active Low).	Unused output. (Do not connect.)
17	NW0 / NC	O	Byte 0 Write Strobe output (Active Low).	Unused output. (Do not connect.)
18	NW1 / NC	O	Byte 1 Write Strobe output (Active Low).	Unused output. (Do not connect.)
19	NW2 / NC	O	Byte 2 Write Strobe output (Active Low).	Unused output. (Do not connect.)
20	NW3 / NC	O	Byte 3 Write Strobe output (Active Low).	Unused output. (Do not connect.)
21	NRD / NC	O	Read Data Strobe output (Active Low).	Unused output. (Do not connect.)
22	ARM_ALE / NC	O	ALE output to the microprocessor (Active High). Controls the transparent latches at the microprocessor address outputs.	Unused output. (Do not connect.)
23	DBE / NC	O	Data Bus Enable output to the microprocessor. When Low, places the microprocessor data bus drivers in a high impedance state.	Unused output. (Do not connect.)
24	ACCUM_INT	O	A free running interrupt to the microprocessor. It allows control of data transfer between the accumulators in the correlator and the microprocessor. It is active Low when configured for ARM System mode or Motorola mode and is active High in Intel mode.	
25	MEAS_INT	O	An interrupt to the microprocessor. It allows control of measurement data transfer between the correlator and the microprocessor. It is active Low when configured for ARM System mode or Motorola mode and is active High in Intel mode.	
26	NBW / WRPROG	I	Byte/Word input from the microprocessor. Low indicates a byte transfer, and High a word transfer.	Write–Read Program input. In Intel mode, High selects 486 style interface and Low 186 style. Unused in Motorola mode
27	NMREQ / DISCIP2	I	Memory Request input from the microprocessor. Low indicates that the microprocessor requires a memory access during the following cycle.	Multi–purpose discrete input.
28	NOPC / NINTELMOT	I	Opcode fetch input from the microprocessor. Low indicates that an instruction is being fetched and High that data is being transferred.	High selects Motorola mode and Low Intel mode.
29	NRW / DISCIP3	I	Read/Write Select input from the microprocessor. Low indicates a read cycle and High a write cycle.	Multi–purpose discrete input.
30	MCLK / NC	O	Microprocessor Clock output (nominally 20MHz). Its phases can be stretched under control of the Microprocessor Interface.	Unused output. (Do not connect.)

Pin No	Signal Name	Type	Description ARM System Mode	Description Standard Interface Mode
31	ABORT/ MICRO_CLK	O	Abort output to the microprocessor. Generates a valid ARM Data Abort sequence, triggered by a rising edge at MULTI_FN_IO if this function is enabled.	20MHz Clock output. Provides a 20MHz clock with a 1:1 mark-to-space ratio
32	DISCIO	I/O	Multi–purpose discrete input / output. After a GP2021 reset it is configured as an input.	
33	A22 / READ	I	Address input from the microprocessor. A<22:20> are decoded to select the address space partitioning.	Read input from the microprocessor. In Intel mode it is the active Low read strobe. In Motorola mode it is the Read (High)/Write (Low) select line.
36	A21 / NCS	I	Address input from the microprocessor. A<22:20> are decoded to select the address space partitioning.	GP2021 Chip Select input (Active Low).
37	A20 / WREN	I	Address input from the microprocessor A<22:20> are decoded to select the address space partitioning.	Write–Read Strobe input from the microprocessor. In Intel mode it is the active Low write strobe. In Motorola mode it is the active High Write-Read strobe.
38 – 45	A<9:2>	I	Address Inputs <9:2> from the microprocessor. These allow register selection.	
46	A1 / ALE_IP	I	Address input 1 from the microprocessor. A<1:0> are decoded to provide individual byte write selection via NW<3:0>.	Address Latch Enable input from microprocessor (Active High)
47	A0 / NRESET_IP	I	Address input 0 from the microprocessor. A<1:0> are decoded to provide individual byte write selection via NW<3:0>.	Reset input (Active Low).
48– 54, 57–65	D<0:15>	I/O	Bidirectional data bus.	
66	PLL_LOCK	I	PLL Lock Indicator input from RF section. When High this signa indicates that the PLL within the RF section is in lock and the master clock inputs have stabilised.	
68	DISCOP	O	Multi–purpose discrete output.	
70	CLK_T	I	Master clock input (40MHz).	
71	CLK_I	I	Inverted Master clock input.	
73	SAMPCLK	O	Sample Clock output to the front end. Provides a 5.714MHz clock with a 4:3 mark–to–space ratio.	
75	NBRAM / DISCIP4	I	Battery Backed RAM select input. Defines the state of the NRAM output in Power Down mode.	Multi–purpose discrete input.
76	SIGN0	I	SIGN0 input from the RF section.	
77	MAG0	I	MAG0 input from the RF section.	
78	SIGN1	I	SIGN1 input from a second, optional, RF section.	
79	MAG1	I	MAG1 input from a second, optional, RF section.	
80	DISCIP1	I	Multi–purpose discrete input.	

Difference between Real and Complex_Input Mode

The input mode is selected by theFRONT_END_MODE bit in the SYSTEM_SETUP register. It defaults to Real_Input mode at power up. The differences between Real and Complex input mode are summarised in the following table.

Description	Real_Input mode	Complex_Input mode
Recommended Master clock frequency	40MHz	35MHz
GP2021 internal clocking [1]	± 7	÷ 6
MICRO_CLK 2 output frequency mark : space	20MHz 1:1	17.5MHz 1:1
Pin No 76	SIGN 0	SIGN_I
Pin No 77	MAG 0	MAG_I
Pin No 78	SIGN 1	SIGN_Q
Pin No 79	MAG 1	MAG_Q
Input Signal Sampling Rate	5.714MHz	5.833MHz
SAMPCLK output frequency mark : space	5.714MHz 4:3	Not available (held Low)

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Notes. 1 The GP2021 interrupt and TIC timebase dividers are clocked by this resulting clock.
2 The MCLK output is derived from this signal. In ARM mode the phases of MCLK are stretched by the Microprocessor Interface block.

FUNCTIONAL DESCRIPTION

The GP2021 incorporates a 12 Channel GPS Correlator, together with microprocessor support functions including a Dual UART, a Real Time Clock and Memory Control Logic for the ARM60 microprocessor. It can be configured for either ARM System mode or Standard Interface mode. A block diagram of the GP2021 is shown in Fig. 3.

Whilst in ARM System mode the Memory Control Logic allows an ARM60 microprocessor to interface with the Correlator, Real Time Clock, Dual UART and a variety of memory devices (i.e. SRAM, EPROM, Flash and EEPROM), without the need for external glue logic.

In Standard Interface mode the GP2021 allows most 16 and 32 bit microprocessors to interface with the Correlator, Real Time Clock and Dual UART. More specifically, this mode allows the interface to be configured for either Intel or Motorola style microprocessor interfaces.

In the functional description which follows the correlator is described first, followed by the peripheral functions.

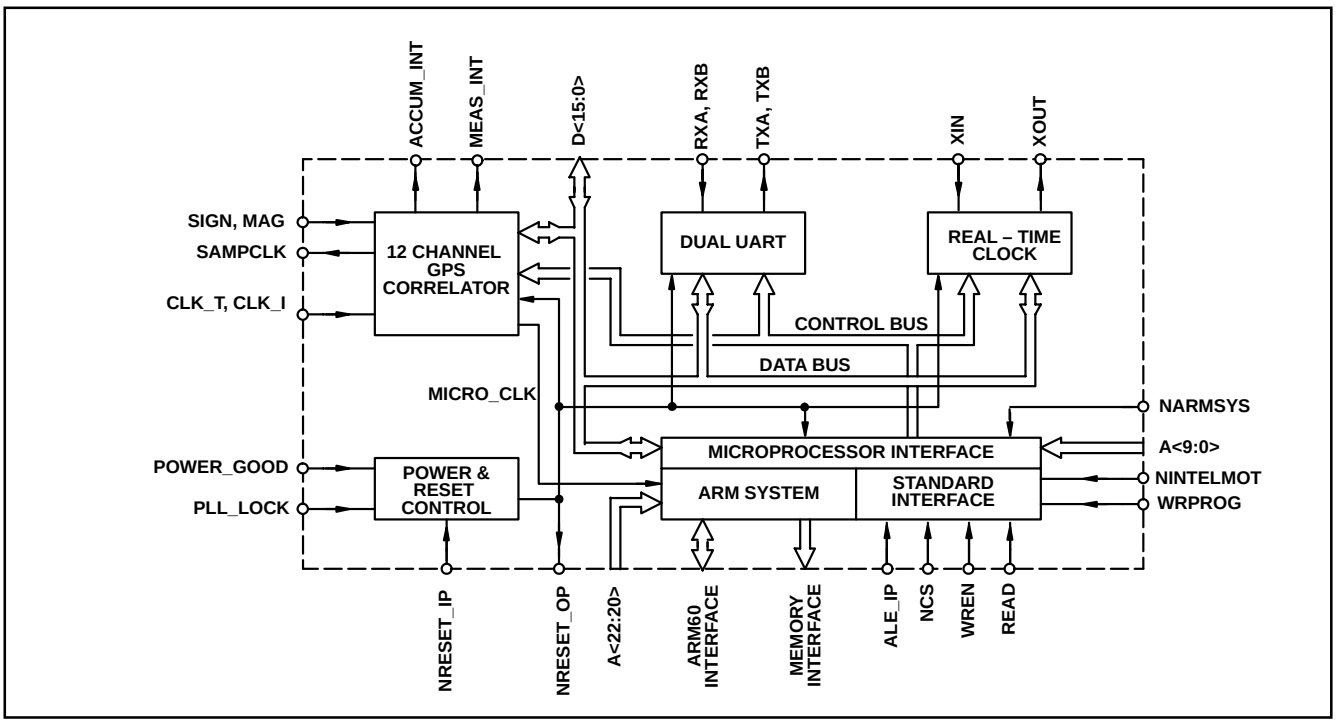


Fig. 3 : GP2021 block diagram

12 CHANNEL CORRELATOR

Fig. 4 shows a block diagram of the correlator. It consists of the following blocks:

Clock Generator

The Clock Generator block divides the frequency of the master clock CLK_T/CLK_I by 6 or 7 to give the internal multi–phase set of clocks. When in Real_Input mode CLK_T/CLK_I will normally be a 40MHz clock, which is divided by 7. When in Complex_Input mode it will normally be at 35MHz which is divided by 6. The SAMPCLK pin is an output giving a 4:3 mark–to–space ratio clock at 40 MHz / 7 (= 5·714MHz) in Real_Input Mode.

The Clock Generator also produces the MICRO_CLK signal at half the master clock frequency (20 MHz for Real_Input mode, 17.5 MHz for Complex_Input mode) with a 1:1 mark–to–space ratio. This signal is output on the MICRO_CLK pin in Standard Interface mode. However, its main purpose is that of a synchronising clock to the memory control logic in ARM System Mode and it is from this that the processor clock output, MCLK, is derived.

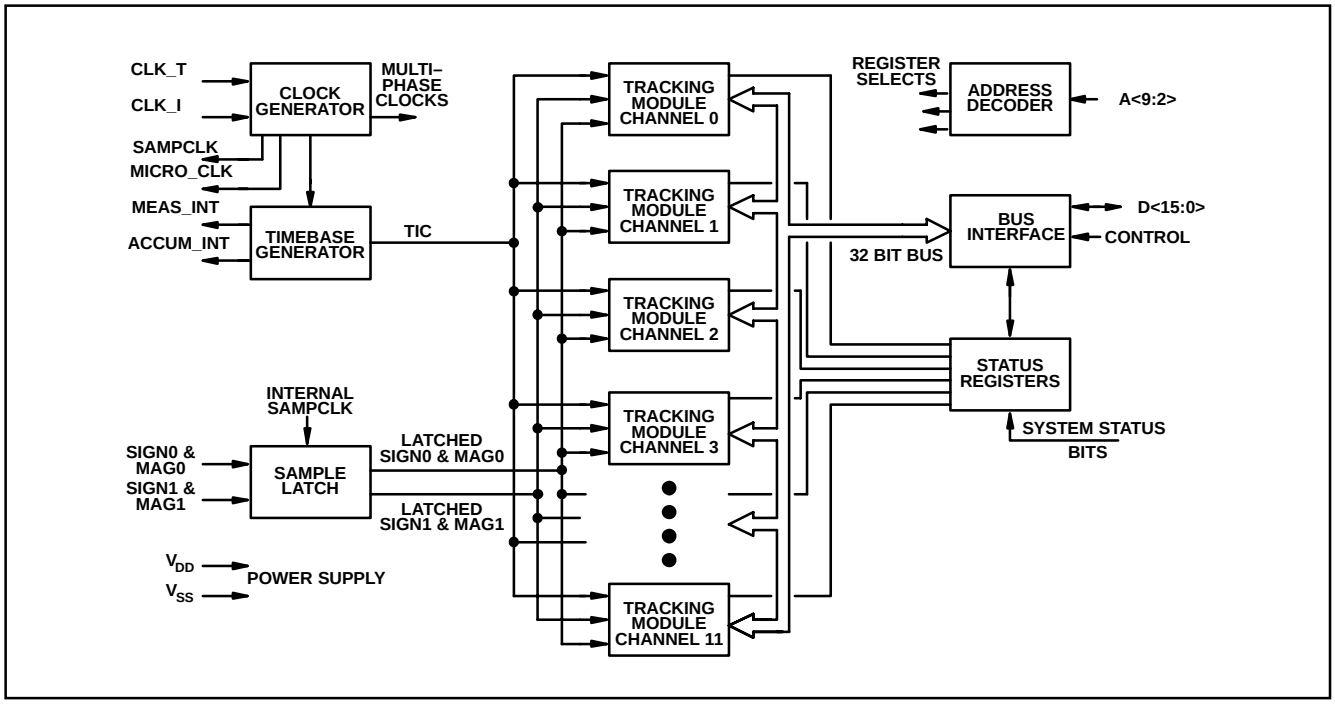


Fig. 4 Correlator block diagram

Timebase Generator

The Timebase Generator produces 4 important timing signals: ACCUM_INT, TIC, MEAS_INT and TIMEMARK. ACCUM_INT is an interrupt provided to control data transfer between the correlator accumulators and the microprocessor. It may be detected by means of the ACCUM_INT output or by reading the ACCUM_STATUS_A register (where bit 15 is a flag indicating that ACCUM_INT has occurred since the previous read of this register). ACCUM_INT is cleared by reading ACCUM_STATUS_A.

After power–up this interrupt occurs every 505.05µs. Its period can subsequently be changed in one of 3 ways:

1) toggling the FRONT_END_MODE bit of the SYSTEM_SETUP register,
2) toggling the INTERRUPT_PERIOD bit of the SYSTEM_SETUP register, or
3) writing directly to the PROG_ACCUM_INT register.

See section ‘‘Detailed Description of Registers” on page 25 for more information.

TIC is an internal signal with a default period of 99999.90µs. It is used to latch measurement data (Epoch count, Code phase, Code DCO phase, Carrier DCO phase and Carrier cycle count) of all 12 channels at the same instant. Its period can subsequently be changed, by writing to the PROG_TIC_HIGH and PROG_TIC_LOW registers, or toggling the FRONT_END_MODE bit of the SYSTEM_SETUP register.

MEAS_INT is a signal derived from the TIC counter. It may be used by the microprocessor as a software module switching interrupt either by using the MEAS_INT output or by reading the ACCUM_STATUS_B or MEAS_STATUS_A register. MEAS_INT is activated at each TIC and 50 ms before each TIC so long as the TIC period is greater than 50 ms. If the TIC period is less than 50 ms, MEAS_INT is activated only at each TIC. It is cleared by reading either the ACCUM_STATUS_B or MEAS_STATUS_A register, depending upon the MEAS_INT_SOURCE bit of the SYSTEM_SETUP register.

TIMEMARK is also derived from TIC and may be output on one of the discrete output pins. This signal is intended to be used as an accurate 1 Pulse Per Second timing reference, aligned to UTC (Universal Time Co–ordinated system), with a pulse width of 1ms.

TIMEMARK has two methods of operation but in both

cases TIMEMARK rising edges are generated co–incident with the rising edges of TIC. Therefore, for TIMEMARK to be aligned with UTC, TIC must be aligned with UTC. This is done by modifying the TIC period for a single TIC cycle, then setting it back to its original value, thus slewing the phase of TIC. TIMEMARK may be generated by setting the TIMEMARK_ARM bit in the TIMEMARK_CONTROL register, in which case the next TIC will generate a rising edge at TIMEMARK and clear the TIMEMARK_ARM bit. Alternatively TIMEMARK may be generated as a programmable integer number of TIC's, again under the control of the TIMEMARK_CONTROL register.

Status Registers

There are four status registers (ACCUM_STATUS_A, _B, _C and MEAS_STATUS_A). These contain flags associated with the accumulated and measurement data held on each of the 12 channels. Some system level status bits also appear in these registers.

Sample Latches

The Sample Latches synchronise data from the front end to the internal SAMPCLK. In Real_Input mode the down converted satellite signal can be sampled at the output of the front end by SAMPCLK. This data is then input to the GP2021 as 2 bit data on either the SIGN0, MAG0, or SIGN1, MAG1 inputs, where it is re–sampled at the next rising edge of SAMPCLK. These signals are then distributed to the 12 tracking modules.

When a GP2015 or GP2010 front end is used, the data represents a band–limited signal at an IF centered on 4.309MHz. Sampling at 5.714MHz aliases it to an IF of 1.405MHz.

In Complex_Input mode, the down converted satellite signal is applied direct to the GP2021 at its SIGN0, MAG0, SIGN1, MAG1 inputs, which act as In–Phase Sign, In–Phase Magnitude, Quadrature Sign and Quadrature Magnitude respectively. These signals are sampled at 5.833MHz within the correlator and then passed to the tracking modules.

Address Decoder

The Address Decoder performs address decoding for the correlator.

Bus Interface

The Bus Interface controls the transfer of data between the external 16 bit wide data bus and the internal 32 bit data bus.

Apart from the code and carrier DCO increment values, all data transfers are 16 bits wide. Write operations to the code and carrier DCO's are 32 bit data transfers, in which the High 16 bit word must be written immediately before the low 16 bit word. Note that the write cycle to write cycle delay of 300 ns referred to in the Microprocessor Interface does not apply between the first and second write cycles for 32 bit DCO data transfers. For further information see the Microprocessor Interface section.

TRACKING MODULES

The Tracking Modules are 12 identical signal tracking channels numbered CH0 to CH11, each with the block diagram shown in Fig 5. These blocks generate the data used to track the satellite signals. There is no overwrite protection mechanism on this data. For further information see the section on CONTROLLING THE GP2021.

Each Tracking Channel can be individually programmed to operate in either Update or Preset mode. Update mode is the normal mode of operation. Preset mode is a special mode of operation where writes to certain registers are delayed until the next TIC to allow synchronisation of registers and presetting of the code DCO phase. For further information see the Preset Mode section in the Detailed Operation of the GP2021.

The individual sub–blocks in the tracking modules are:

Carrier DCO

The Carrier DCO, which is clocked at the SAMPCLK frequency, is used to synthesise the digital local oscillator signal required to bring the input signal to baseband in the mixer block, and must be adjusted away from its nominal value to allow for Doppler shift and reference frequency error.

When used with the GP2015/GP2010 the nominal frequency of this signal is 1·405396825 MHz (with a resolution of 42.57475 MHz) and is set by loading the 26 bit register CHx_CARRIER_DCO_INCR. This very fine resolution is needed so that the DCO will stay in phase with the satellite signal for an adequate time. The Carrier DCO Phase cannot be directly set, but must be adjusted by altering the frequency.

The Carrier DCO outputs are 4 level, 8 phase sinusoidals with the following sequences over one cycle:

Destination Arm	Sequence
I_{LO}	–1+1+2+2+1–1–2–2
Q_{LO}	+2+2+1–1–2–2–1+1

Table 1 Carrier DCO outputs

As the clock to the DCO is normally less than 8 times the output frequency, not all phases are generated in every cycle. With a typical clock frequency of 5·714 MHz and an output frequency of 1·405 MHz there are only around 4 phases per cycle. These will slide through the cycle as time progresses to cover all values.

Code DCO

The Code DCO is similar to the Carrier DCO block. It is also clocked at the SAMPCLK frequency and synthesises the oscillator required to drive the code generator at twice the required chipping rate. The nominal frequency of the output is 2·046 MHz, to give a chip rate of 1·023 MHz and is set by loading the 25 bit register CHx_CODE_DCO_INCR.

It is programmed with a resolution of 85·14949 mHz when used with a GP2015/GP2010 front end. The very fine resolution is again needed to keep the DCO in phase with the satellite signal. The Code DCO Phase can only be set to the exact satellite phase in Preset mode. In Update mode, it must be aligned with the satellite phase by adjusting its frequency.

Carrier Cycle Counter

The Carrier Cycle Counter is 20 bits long, and keeps a count of the number of cycles of the Carrier DCO between TIC's. This is not needed for a basic navigation system but may be used to measure the range change (delta–range) to each satellite between TIC's. The delta ranges can be used to smooth the code pseudo–ranges. For finer detail the Carrier DCO phase may also be read at each TIC to give the fractional part of the cycle count or delta–range.

C/A Code Generator

The C/A Code Generator generates the selected Gold code for a GPS satellite (1 to 32), a ground transmitter (pseudolite, 33 to 37), an INMARSAT–GIC satellite (201 to 211) or a GLONASS satellite. A Gold code is selected by writing a specific pattern of 10 bits, as listed in the section 'Detailed Description of Registers', to the CHx_SATCNTL register, or by setting the GPS_NGLON bit to Low for the GLONASS code. Two outputs are generated to give both a PROMPT and a TRACKING signal. The TRACKING signal can be set to one of four modes: EARLY (one half chip before the PROMPT signal), LATE (one half chip behind), DITHERED (toggled between EARLY and LATE every 20ms) or EARLY–MINUS–LATE (the signed difference).

The output code is a sequence of +1's and –1's for all code types except EARLY–MINUS–LATE where the result can also

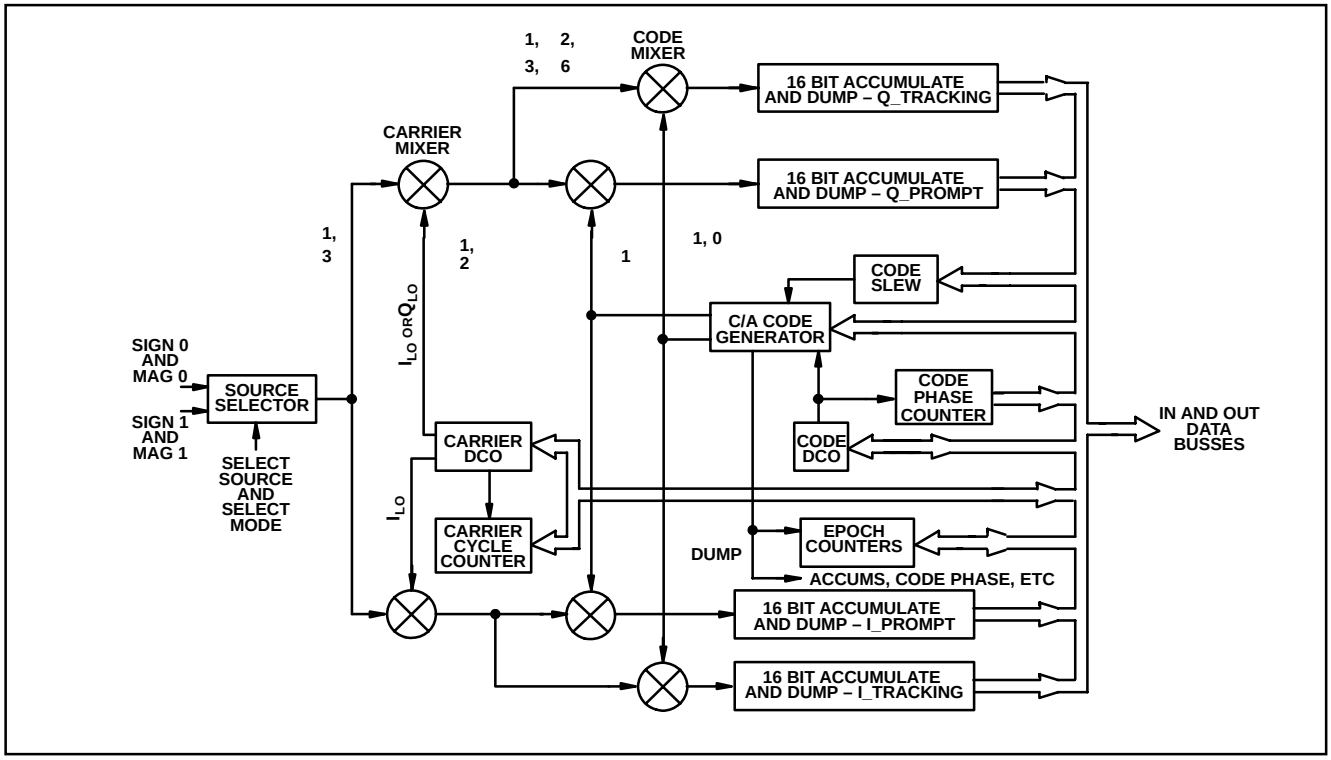


Fig.5 Tracking Module block diagram

be a 0. To avoid having an unused LSB in the accumulators, the values in EARLY–MINUS–LATE mode are halved from the +2, 0, –2 that results from the calculation (+1 or –1) – (+1 or –1) to +1, 0, –1. This must be considered when choosing thresholds in the software, as the correlation results will be exactly half of the values otherwise expected.

At the end of every code sequence (1023 chips in GPS mode or 511 chips in GLONASS mode) a DUMP signal is generated to latch the Accumulated Data for use by the signal tracking software. Each channel is latched separately, as the satellite signals are not received in phase with each other.

Source Selector

In Real_Input mode the Source Selector selects which input signal pair to use (SIGN0/MAG0 or SIGN1/MAG1). In Complex_Input mode SIGN0/MAG0 are passed to the In–phase arm and SIGN1/MAG1 to the Quadrature arm. The data is treated as having the values shown in Table 2 below (in both modes):

Sig	Mag	Value
0	1	-3
0	0	-1
1	0	+1
1	1	+3

Table 2 SIGN/MAG values

Carrier Mixers

The Carrier Mixers multiply the digital input signal by the Carrier DCO digital local oscillator to generate a signal at baseband. In Real_Input mode both I and Q Carrier DCO phases are directed to the appropriate mixers. In Complex_Input mode a single In–Phase Carrier DCO output is used in both mixers since the input signal is already in I and Q form. The mixing of the Carrier DCO outputs with the input signal produces a baseband signal which can have the values ±1, ±2, ±3 and ±6.

Code Mixers

The Code Mixers multiply the I and Q baseband signals from the Carrier Mixers with both the PROMPT and TRACKING local replica codes to produce 4 separate correlation results. The correlation results are passed to the Accumulate and Dump blocks for integration.

Accumulate and Dump

The Accumulate and Dump blocks integrate the Mixer outputs over a complete code period of nominally 1ms.

There are 4 separate 16 bit accumulators for each channel. These represent the correlation of the I and Q signals with the PROMPT and TRACKING codes, over the integration period. There is no overwrite protection mechanism on these registers so the data must be read before the next DUMP.

Code Phase Counter

The Code Phase Counter counts the number of half–chips of generated code and stores this value in the CHx_CODE_PHASE register on each TIC.

Code Slew Counter

The Code Slew Counter is used to slew the generated code by a number of half chips in the range 0 to 2047. In Update mode the slew occurs following the next DUMP. In preset mode it occurs at the next TIC. All slew operations are relative to the current code phase. The Code Slew counter must be written to each time a slew is required.

During the slewing process the accumulators for the channel being slewed are inhibited so that the first result is valid. If a slew is written while a channel is disabled it will occur as soon as the channel is enabled.

Epoch Counter

The Epoch Counters keep track of the number of code periods over a 1 second interval. This is represented by a 5 bit word for the number of 1 ms integration periods (0 to 19), plus a 6 bit word containing the number of 20 ms counts (0 to 49). The Epoch Counters can be pre–loaded to synchronise them to the data stream coming from the satellite. This value will be transferred immediately to the counter when in Update mode, or after the next TIC if in PRESET Mode.

The Epoch Counter values are latched on each TIC into the CHx_EPOCH register. In addition the instantaneous values are available from the CHx_EPOCH_CHECK register.

PERIPHERAL FUNCTIONS

The following section describes the Dual UART, Real Time Clock and Watchdog, Power and Reset Control and Discrete I/O blocks.

Dual UART

A Dual UART is included for serial communications. It has 2 identical blocks, UART_A and UART_B, each containing separate transmit and receive channels. The parity and separate transmit and receive baud rate can be configured independently for each UART. Each uses a polled processor interface and each transmit and receive channel has an 8 byte deep FIFO.

For further information on the UART registers refer to the Detailed Description of Registers and the GP2021 Register Map.

A typical serial data stream is shown in Fig. 6. The Parity bit is optional and if no parity is selected the time slot for it is removed from the data stream and the Stop bit follows immediately after the last data bit in both transmit and receive directions. Note that the LSB is always preceded by a Start bit. Table 3 shows possible UART configurations.

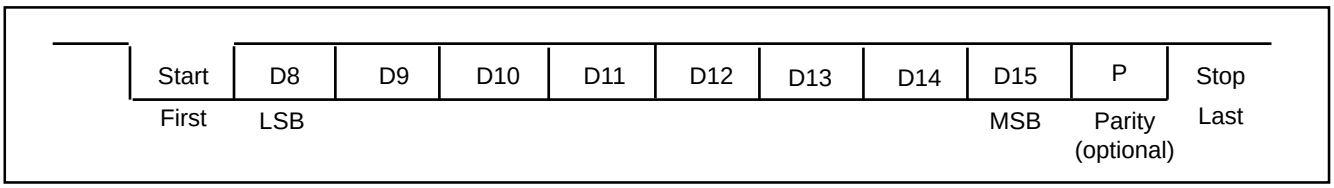


Fig. 6 Serial Data waveform

Parameter	Value
Start bits	1 bit Low
Data bits	8 bits Logic 0 = Low Logic 1 = High
Stop bits	1 bit High
Parity	Odd/Even/None
Flow control	None
Transmit FIFO depth	8 bytes
Receive FIFO depth	8 bytes
FIFO speed	Transmit FIFO write rate and Receive FIFO read rate maximum is one byte per 230ns. The maximum buffer through delay is 2 µ s.
Data rate	300, 600,1.2k, 2.4k, 4.8k, 9.6k, 19.2k, 38.4k and 76.8k baud. Transmit and Receive rates individu-ally configured.

Table 3 UART Functionality

Receiver

The incoming data streams on RXA, RXB are sampled by a clock at nominally 20 times the data rate, to search for an incoming Start bit. Once the receiver is synchronised to the data stream, each data bit is sampled only at its nominal centre to avoid errors due to slow or noisy bit edges. The receiver will resynchronise to each Start bit to prevent the accumulation of phase errors.

Only valid data (having correct Start, Stop and Parity bits) will be stored in the receiver FIFO. If a received word contains a parity or framing (Start/Stop bit) error, the appropriate flag bit will be set in the status register. If too many valid data words are received for the FIFO to hold, the excess will not be written into the FIFO, and an Overflow bit will be set in the status register. When receiving a continuous transmission, the Start bit of one word will follow immediately after the Stop bit of the preceding word. At lower word rates, a High is expected between words. The receiver will accept data with a baud rate error of up to ±1%.

Transmitter

Data is transmitted on pins TXA and TXB. In continuous transmission, the Start bit of one word will follow immediately after the Stop bit of the preceding word. At lower word rates, a High is sent between words.

If too many data words are written by the microprocessor to the UART for the transmitter FIFO to hold, the excess will not be stored. The UART will resume normal operation as soon as space becomes available. To avoid data loss, the software should limit the transmit data rate by either: keeping track of the number of bytes sent and the time to transmit them, or should read the Status register and stop writing when the Full bit is set.

Reset

It is possible for the software to reset either UART independently via the RESET_CHx registers. A hardware reset affects both UARTs. During a UART reset, the contents of all Control, and Status registers will be cleared. In addition the Transmit and Receive FIFO's will be emptied and the TX outputs will be held Low.

Channel Loopback

For system test purposes, a loopback facility is provided for each channel, controlled by the Configuration registers. In loopback, the TX output is set High.

Real Time Clock (RTC) and Watchdog

This block consists of a 32.768kHz crystal oscillator, a fixed divider, a 24 bit counter, a Watchdog function and three 8 bit data registers. XIN and XOUT are the crystal in and crystal out connections to the oscillator circuit. A recommended crystal oscillator circuit is shown in Fig. 7. When the Real Time Clock $\underline{ss}$ is not being used, XIN must be tied Low.

The first divider is a fixed divide by 32768 giving a 1 Hz output. The counter then counts seconds, giving a maximum time of 194 days. The time is output in three 8 bit registers with the data being latched when a read is performed to the LS register (The register holding the least significant byte of the clock data). On reaching its maximum count, the count is frozen (i.e. all 1's), until being reset.

In Power Down mode the Real Time Clock continues to run, but access to the data registers is not allowed. When normal power is restored, the software can determine the elapsed time whilst in Power Down mode, thereby assisting in estimating the current position of GPS satellites and so reducingTime–To–First–Fix.

The Watchdog generates a System Reset (see Power And Reset Control) if the Watchdog Reset address has not been written to for a period of approximately 2s. The watchdog function is inhibited whilst in Power Down mode and can be disabled via a bit in the System Configuration register.The software is able to reset the Real Time Clock and Watchdog via the Clock Reset and Watchdog Reset registers respectively. In addition the watchdog is reset during a System Reset.

For further information on the registers refer to the section Detailed Description of Registers.

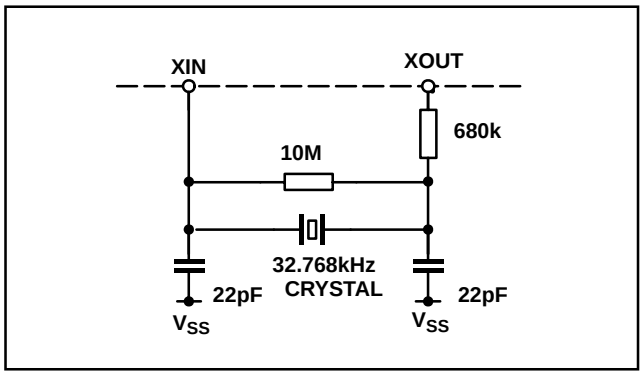


Fig. 7 Recommended Crystal Oscillator Circuit

Power and Reset Control

This block performs 2 functions: Power Control and System
Reset Generation

Power Down Mode

In order to allow power conservation within a battery backup system, the GP2021 provides a Power Down mode, in which the supply voltage may drop to a minimum of 2.2V, thereby minimising the supply current. In this mode all functions within the GP2021 are disabled except for the Real Time Clock.

The GP2021 is placed in Power Down mode by taking the POWER_GOOD pin Low. In ARM System mode with the NBRAM pin held Low, the initiation of Power Down mode is delayed until just after a falling edge of MICRO_CLK so as not to corrupt battery backed RAM. Fig. 8 shows a suggested circuit implementation. Table 4 shows output logic levels in Power Down mode.

In Power Down mode all inputs and I/Os except POWER_GOOD and XIN are internally switched to known logic levels to prevent extraneous switching from causing excessive power consumption, and may therefore be left floating. All the I/O pins (D<15:0>, MULTI_FN_IO and DISCIO) have their output drivers driven to the High Impedance state.

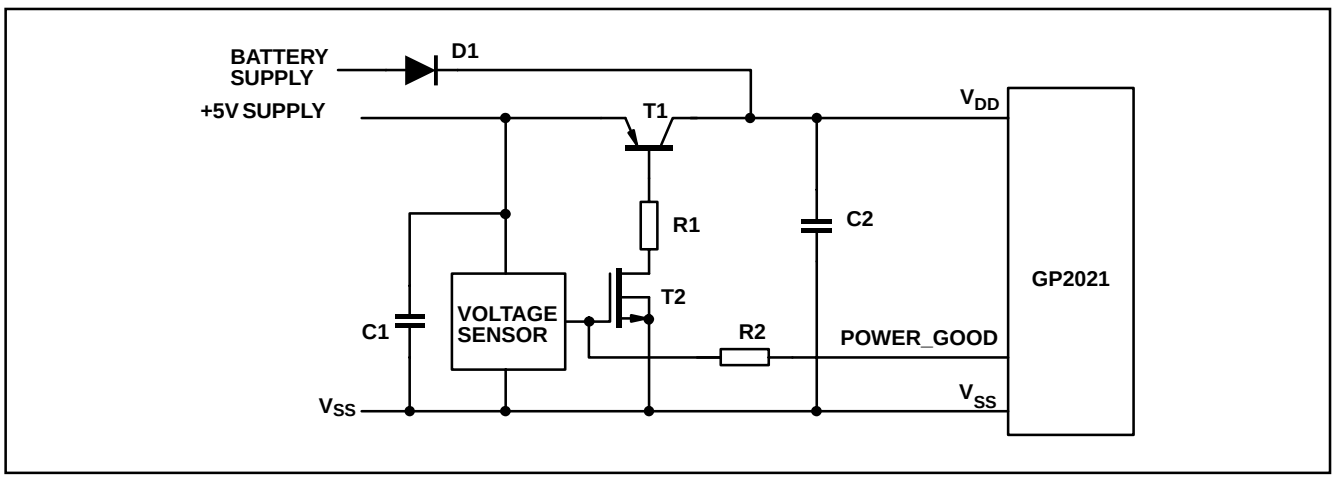


Fig. 8 : Suggested Battery Backup Configuration

Pin Name	Logic Level
NW<3:0> / NC	Low
NRD / NC	Low
NRAM (standard interface mode)	Low
NRAM (ARM system mode)	$\overline{\text{NB RAM}}$
NROM / NC	High Impedance
NSPARE_CS/NC	High Impedance
NEEPROM / NC	High Impedance
TXA,TXB	Low
ACCUM_INT	High Impedance

Pin Name	Logic Level
MEAS_INT	**High Impedance**
ABORT / MICRO_CLK	Low
MCLK / NC	Low
ARM_ALE / NC	Low
DBE / NC	Low
NRESET_OP	Low
DISCOP	High Impedance
SAMPCLK	Low
XOUT	Active

Table 4 : Output Logic Levels in Power Down Mode

Hardware Reset Generation

The manner in which a hardware reset occurs depends on whether the GP2021 is in ARM System mode or Standard Interface mode. During a hardware reset, the NRESET_OP pin is taken Low and the reset signal is applied within the GP2021 to all blocks except the Real Time Clock.

There are 3 sources of hardware resets common to both ARM System and Standard Interface modes, with an additional source in Standard Interface mode:

POWER_GOOD: A hardware reset will occur if this pin is taken Low, as shown in Fig. 9. The purpose of this input is to detect a power failure. If the NBRAM pin is held Low in ARM System mode, the internal Power Down mode is not entered until about 6ns after the falling edge of MICRO_CLK, otherwise it is entered immediately. This allows for RAM write cycles to complete sensibly when Battery Backed–Up RAM is used, with no corruption of RAM data.

Watchdog: An expiry of the watchdog will result in a hardware reset as shown in Fig. 10. This reset will clear the watchdog whose time–out period is 2–3 seconds.

PLL_LOCK: The PLL_LOCK pin is used to indicate (when High),that the phase locked loop in the RF front end, which generates the master clock, is in lock. This signal is filtered within the GP2021 and the reset state associated with it is only de–activated if the PLL_LOCK input has been high for approximately 50 ms as shown in Fig. 11.

NRESET_IP: In addition to the 3 reset sources described above, an active Low NRESET_IP pin is available in Standard Interface mode if the system resets are to be generated externally. Fig. 12 shows a NRESET_IP generated reset.

Note that the NRESET_OP pin will go High 4 MICRO_CLK cycles after all hardware reset sources have cleared. This fulfills the reset requirements of the ARM60 microprocessor. For information on the state of the registers following a hardware reset refer to the Detailed Description of Registers section.

System Error Status Register

This allows the software to determine whether the source of a hardware reset was from a power failure, a PLL_LOCK failure, watchdog timeout or from an external reset in Standard Interface mode. For further information refer to the Detailed Description of Registers section.

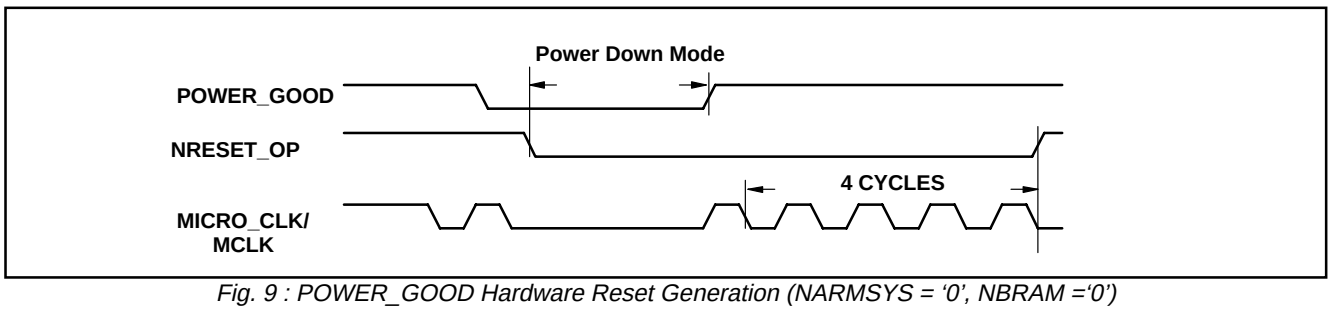


Fig. 9 : POWER_GOOD Hardware Reset Generation (NARMSYS = '0', NBRAM ='0')

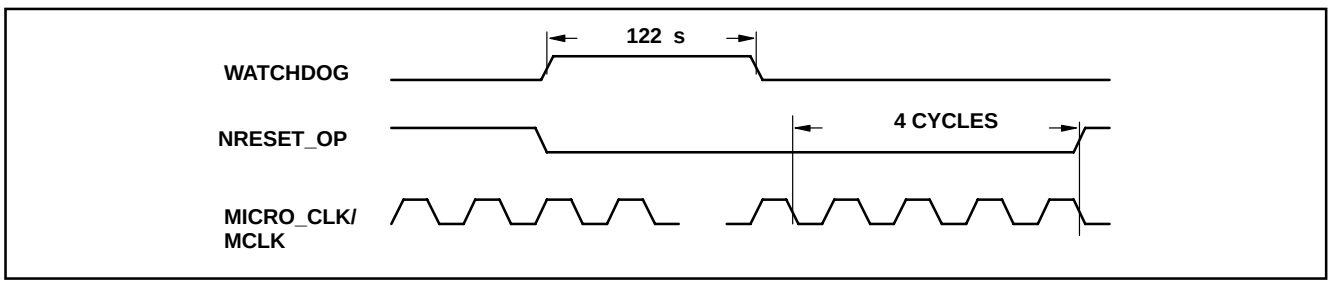


Fig. 10 : Watchdog Hardware Reset Genera-

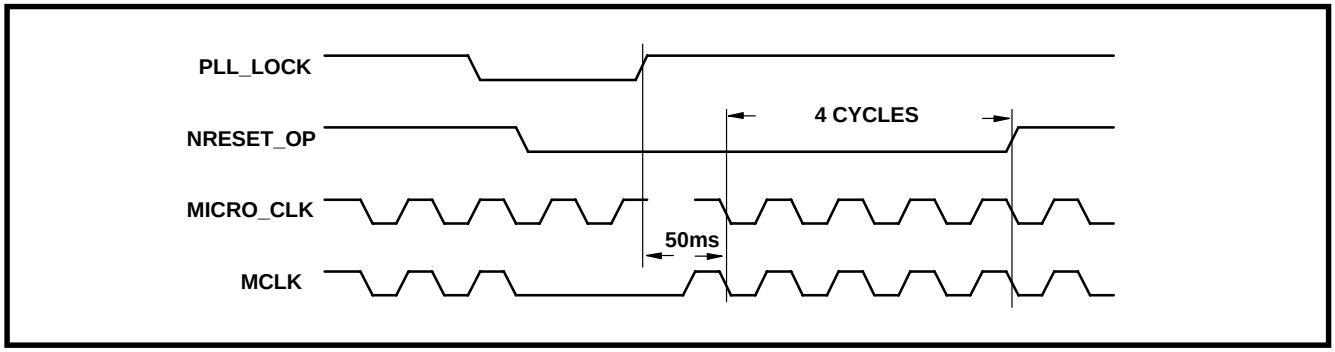


Fig. 11 : PLL_LOCK Hardware Reset Generation

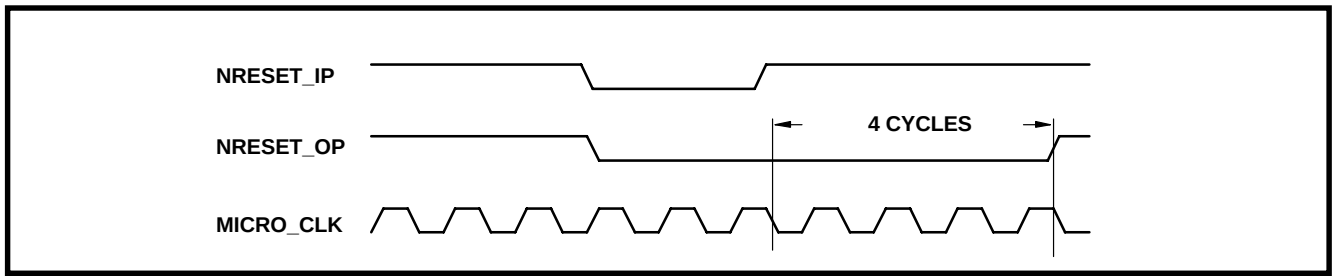


Fig. 12 : NRESET_IP Hardware Reset Generation

Discrete I/O

The GP2021 contains a number of pins which may be used as discrete inputs or discrete outputs for general purpose system monitoring and control applications. The actual pins which may be used for each function vary according to the application and the interface mode of the GP2021.Table 5 shows a list of possible discrete inputs and outputs and the modes in which they may be used. The level on all discrete inputs can be read from the IO_CONFIG register. The status of the DISCIP pin may also be read from ACCUM_STATUS_B. The discrete outputs are controlled via either the SYSTEM_SETUP or IO_CONFIG registers.

Discrete Inputs		
Pin Name	**Read Location**	**Conditions for use as Discrete Input**
NRW/DISCIP3	IO_CONFIG	Standard Interface mode.
NOPC/NINTELMOT	IO_CONFIG	ARM System mode (debug disabled).
NMREQ/DISCIP2	IO_CONFIG	Standard Interface mode.
NBW/WRPROG	IO_CONFIG	Motorola mode only.
DISCIO	IO_CONFIG	DISCIO configured as discrete Input.
NBRAM/DISCIP4	IO_CONFIG	Standard Interface Mode.
MULTI_FN_IO	IO_CONFIG	MULTI_FN_IO configured as discrete input.
SIGN0, MAG0	IO_CONFIG	Single real input mode (GP2010 or GP2015) front end using SIGN0, MAG0.
SIGN1, MAG1	IO_CONFIG	Single real input mode (GP2010 or GP2015) front end using SIGN1, MAG1.
DISCIP1	IO_CONFIG ACCUM_STATUS_B	Always available – dedicated Discrete Input.
RXA	IO_CONFIG	UART Channel A not used.
RXB	IO_CONFIG	UART Channel B not used.
Discrete Outputs		
Pin Name	**Configuration Location**	**Possible Outputs**
DISCOP	SYSTEM_SET_UP	High, Low, CH0 Dump, TIMEMARK, 100kHz Square Wave, Scan Out.
DISCIO	IO_CONFIG	High, Low, TIMEMARK, 100kHz Square Wave.
MULTI_FN_IO	IO_CONFIG	High, Low, TIMEMARK, 100kHz Square Wave.

Table 5 : Discrete Input/Output Configuration

Digital System Test Interface

The GP2021 contains a Digital System Test mode to allow testing of the digital section of the system board. Provided that the MULTI_FN_IO pin is High, this mode is enabled subsequent to a hardware reset or a write of specific data to the IO_CONFIG register. The enabling of Digital System Test mode has 3 effects:

(1) The master clock inputs, CLK_T and CLK_I, are replaced by the signal on the RXA pin. This allows the GP2021 to be clocked synchronously with the board tester which is relevant in ARM System mode where the GP2021 produces the main processor clock to the ARM60.

(2) The RXB pin becomes the active High RTC Reset input. This is mainly intended for factory testing of the GP2021, allowing the RTC to be reset on power up, but may also be used to disable the RTC and Watchdog circuits in this mode.

(3) The PLL_LOCK input and its associated 50ms delay as a reset source is overridden. This removes the dependency on the presence of the front end circuit.

MICROPROCESSOR INTERFACE

The Microprocessor Interface of the GP2021 is compatible with most 16 and 32 bit microprocessors. It can be configured for either ARM System mode or Standard Interface mode by means of the NARMSYS pin.

In Standard Interface mode, two mode control pins NINTELMOT and WRPROG are provided. NINTELMOT selects between Intel and Motorola style interfaces, with WRPROG selecting either Intel i486 or 80186 style interfaces. See Table 6 for more details.

NARMSYS	NINTELMOT	WRPROG	Mode	Processor
0	x	x	ARM System	ARM60
1	1	x	Standard Interface	Motorola style
1	0	0	Standard Interface	Intel 80186 style
1	0	1	Standard Interface	Intel 486 style

Table 6 Microprocessor Interface Configuration.

General Interface Timing

In addition to the detailed timings associated with individual read and write cycles (see Electrical Characteristics section), the internal architecture of the correlator also imposes limits on cycle to cycle timings (in particular write to write cycle and write to read cycle). For a simple microprocessor interface, it must be ensured that no attempts are made to access the correlator for the 300ns following the end of a correlator write cycle in Real_Input mode, or 314ns in Complex_Input mode. However, if the controlling software is to be allowed to write rapidly to the correlator (e.g. block writes), then a more complex bus interface (which inserts wait states) will be required. Note that this limitation only applies after correlator writes, not peripheral function writes, and also does not apply to writes to the correlator X_DCO_INCR_HIGH address.

The correlator section of the GP2021 uses a multi–phase clock internally, and the correlator registers load on specific clock phases. At the end of a write cycle, the falling edge of the internal write strobe latches both the relevant address and data bits. This data is then loaded from the internal data bus to the relevant register at some time during the following 300ns for Real_Input mode or 314ns for Complex_Input mode. A write cycle to the Correlator with no writes in the preceding 300ns (314ns) may be performed immediately, so long as the detailed signal timings are met. However, subsequent read or write cycles to the Correlator after this write cycle may need to be delayed if they would modify the internal address or data lines. Correlator read cycles with no write cycles in the preceding 300ns (314ns) are self–contained, and do not delay subsequent cycles. An isolated read cycle requires only sufficient wait states to meet the detailed signal timings.

Write Cycle To Read Cycle Timings

As described previously, the internal write cycle of the Correlator takes 300ns (314ns). Only once the write cycle is complete will the correlator address decoders switch to decoding the current address. The correlator uses a pre–charged internal data out bus and hence the decoded address lines must be stable before the internal bus drivers are enabled (when the read strobe goes high). Consequently, the read strobe must be held Low until some time after the end of the 300ns (314ns) internal write cycle, to allow sufficient internal address setup time. For the exact timing requirements see the Electrical Characteristics Section.

Write Cycle To Write Cycle Timings

The internal write cycle of the correlator takes 300ns (314ns) after the falling edge of the write strobe. During this time the write internal address and data busses (latched by write) must not be modified. If a second write follows the first, the second write cycle must be delayed such that it ends no earlier than 300ns (314ns) after the end of the previous write. The ‘end’ being a falling edge on the internal write strobe. The specific interface signal timings must also be met.

Notes about Interface Timing Constraints

It should also be noted that these timings need only be met for correlator accesses, not support function accesses, since these utilise self–contained write cycles and are not clocked by the multi–phase clocks. In addition, writes to the Correlator register X_DCO_INCR_HIGH need not incur subsequent delays since writes to this location do not instigate an internal write cycle. A write to this address must always be followed by a write to either a CHX_CARRIER_DCO_INCR_LOW or a CHX_CODE_DCO_INCR_LOW register and it is this second associated write which instigates the internal write cycle.

In ARM System mode all these timing requirements are handled by the internal memory manager.

Note that the exact number of wait states which need to be inserted after a correlator write is not fixed. If the processor were to perform a correlator write then spend 400ns accessing a different peripheral, subsequent correlator reads and writes would incur no additional delay. It is anticipated that correlator wait states will be generated by either one or two external counters, preset on the falling edge of a correlator write, and which then count down to zero. Only once the counter has reached zero may the next correlator access either complete (write) or start (read).

A series of correlator reads and writes are shown in Fig.13.

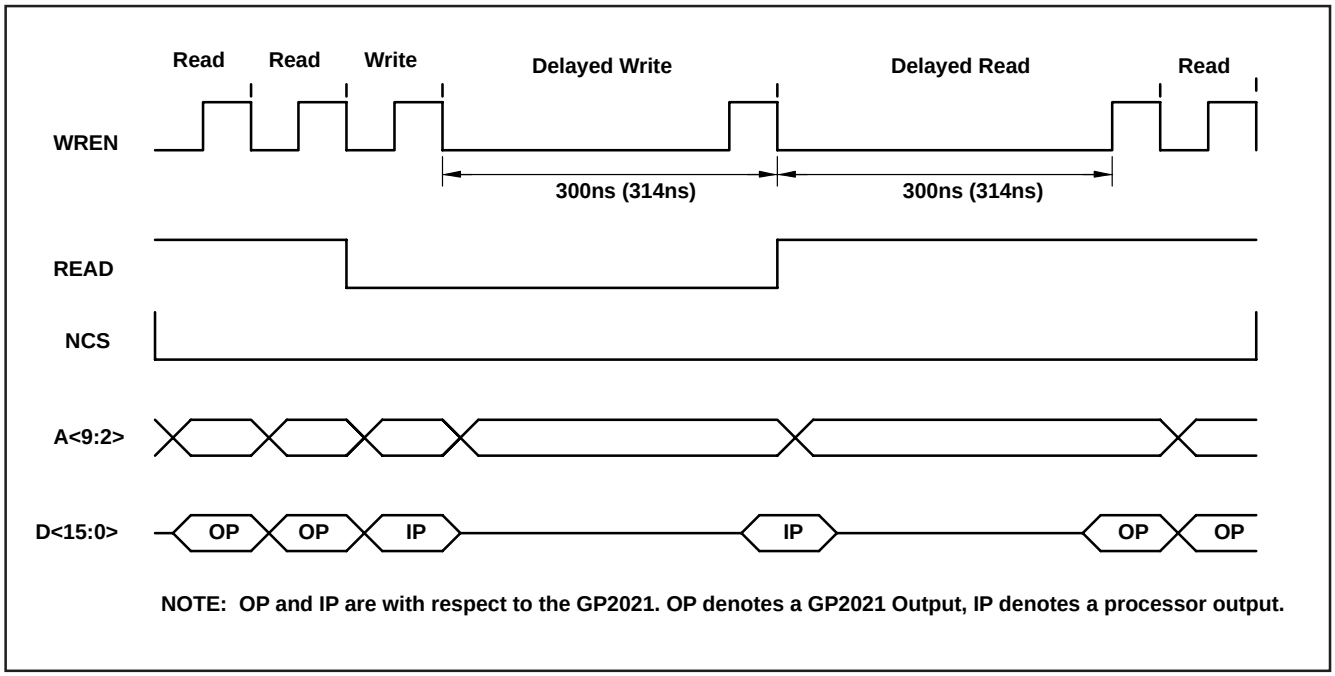


Fig.13 Correlator Bus Timing - Write to Write and Write to Read Timings

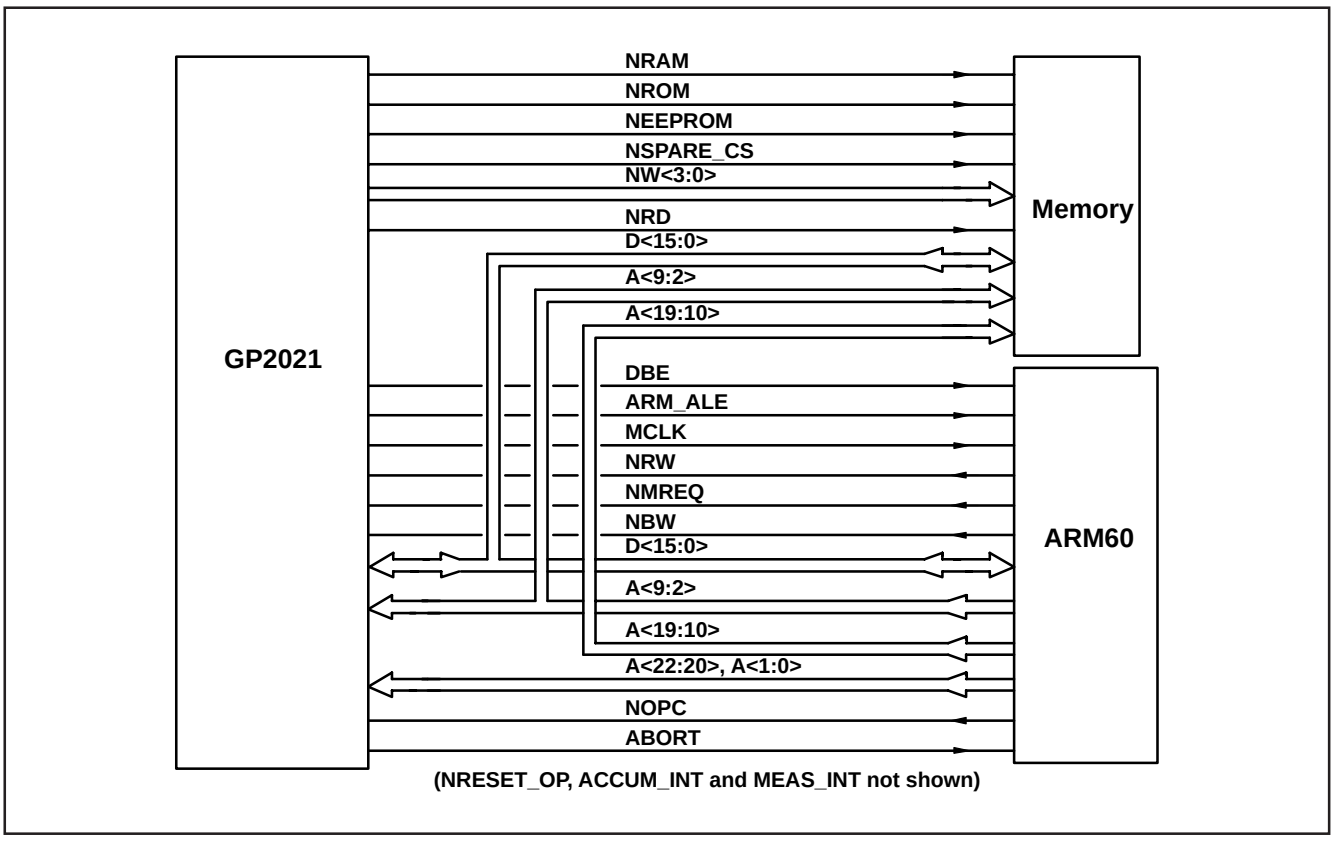


Fig.14 ARM System Mode

ARM System Mode

ARM System Mode, as shown in Fig 14, allows the GP2021 to be interfaced with an ARM60 microprocessor and external memory devices (i.e RAM, ROM, EEPROM, EPROM, Flash) without the need for external glue logic.

Address Map

Both the GP2021 and external memory devices are memory mapped into 1 Mbyte segments by A<22:20> as shown in Table 7.

A22	A21	A20	Device selected	Decoded output pin
0	0	0	ROM	NROM
0	0	1	RAM	NRAM
0	1	0	Correlator	
0	1	1	Support functions	
1	0	0	EEPROM	NEEPROM
1	0	1	User defined	NSPARE_CS
1	1	0	Not Decoded	
1	1	1	Not Decoded	

Table 7 ARM system map

The ARM60 is able to perform either byte or word (4 bytes wide) writes to memory. All registers within the GP2021 are word aligned, with only write accesses to external RAM being either byte or word aligned. The signal NBW is used to indicate either a byte or word write request, with A<1:0> performing byte selection.

Decoding of NBW and A<1:0> is performed by the Microprocessor Interface, with NW<3:0> being the byte write select outputs to memory. During a word write all four of the outputs NW<3:0> will be active.

Note that the register addresses for the Correlator and Support Functions are as shown in the GP2021 Register Map.

Control Signals

The GP2021 uses the ARM60 control signals NBW, NMREQ and NRW to generate the processor clock MCLK and the control signals ARM_ALE and DBE to match the timing requirements of the various memory devices .

The memory interface is via the memory chip select lines (NRAM, NEEPROM, NROM and NSPARE_CS) , the Read line (NRD) and the byte write select outputs (NW<3:0>).

ARM System Timing

The GP2021 timing diagrams for each of the memory interfaces (EEPROM, RAM, ROM, SPARE), and ARM60 areshown in the section Electrical Characteristics.

Wait State Generation

To allow access to slow peripherals or memory, the clock (MCLK) to the ARM60 microprocessor may be stretched in either Phase 1 (Low) or Phase 2 (High), thus allowing wait states to be introduced (where a wait state is defined as being one MCLK period long).

The GP2021 introduces one wait state for accesses to the Real Time Clock, Dual UART and System Control registers, as shown in Fig 15. Correlator accesses, as shown in Fig 19 incur one wait state; subsequent accesses being prevented from contravening the Correlator requirements (see Correlator Functional Description) by adding several wait states.

In order to ensure compatibility with variety of memory devices, the ROM interface is programmable with between one to three wait states, while the EEPROM and SPARE interfaces can be programmed with between three to six wait states via the Wait State Register. For further information on the Wait State Register, refer to Detailed Description of Registers. Read and write cycles for the RAM, EEPROM (or Spare) and ROM interfaces are shown in Figs 16–18.

During a read cycle from Flash Memory, the output disable to data bus release time, could be greater than 25 ns. Hence in order to avoid bus contention, the nominal period of MCLK is stretched by 25 ns during the following cycle.

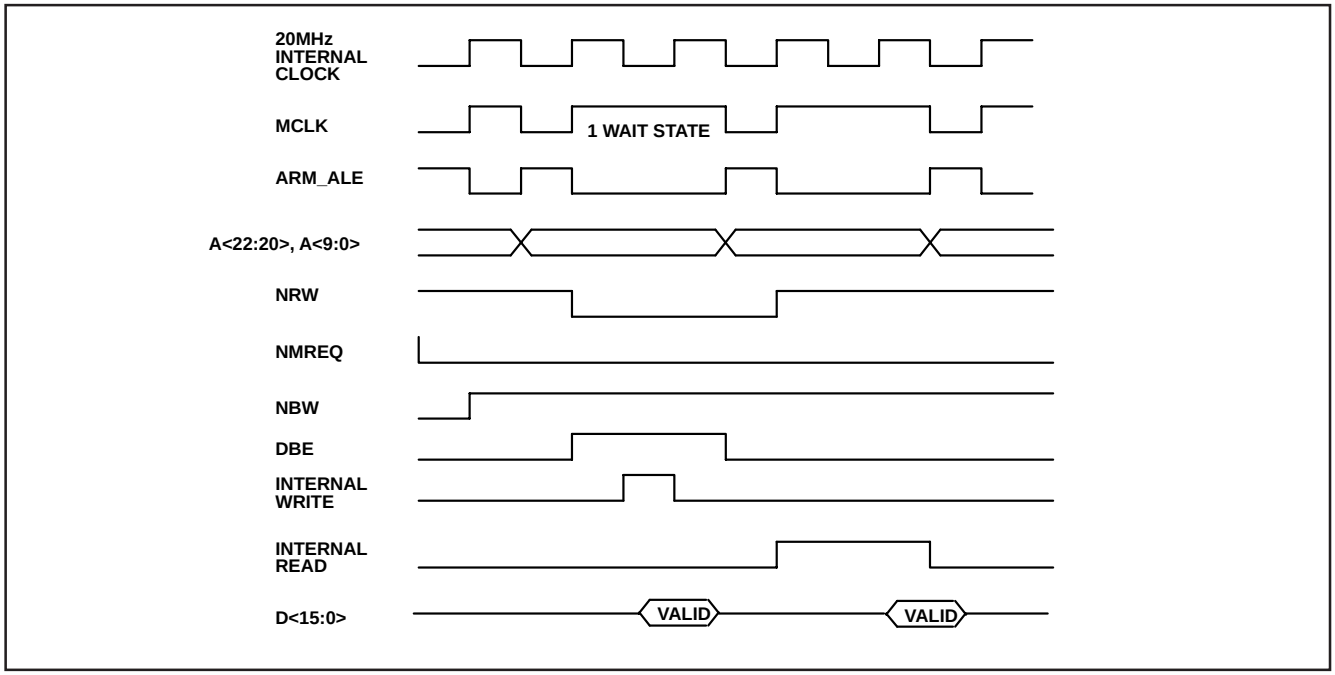


Fig.15 Peripheral functions write/read Cycle

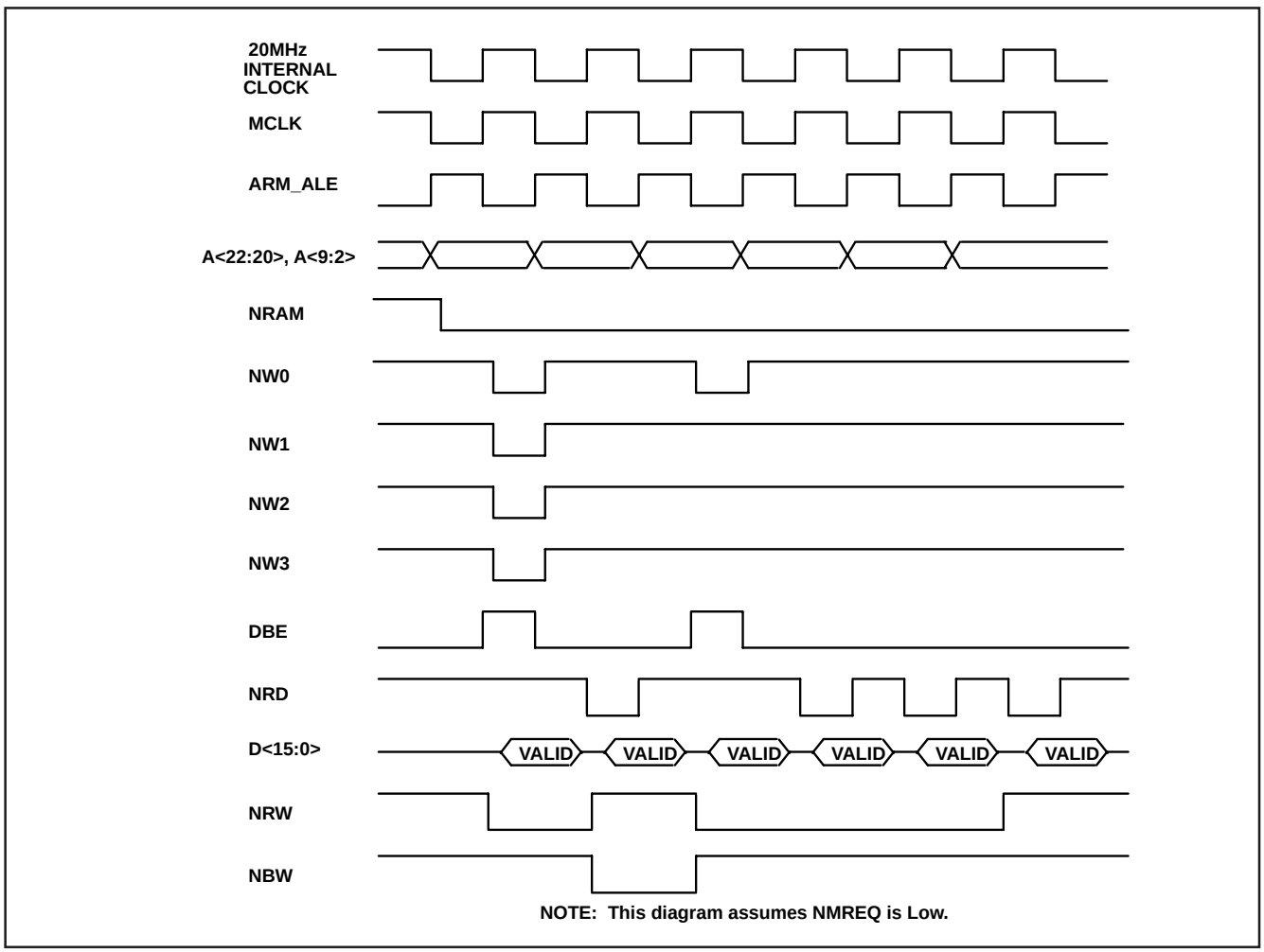


Fig.16 RAM read/write Cycle

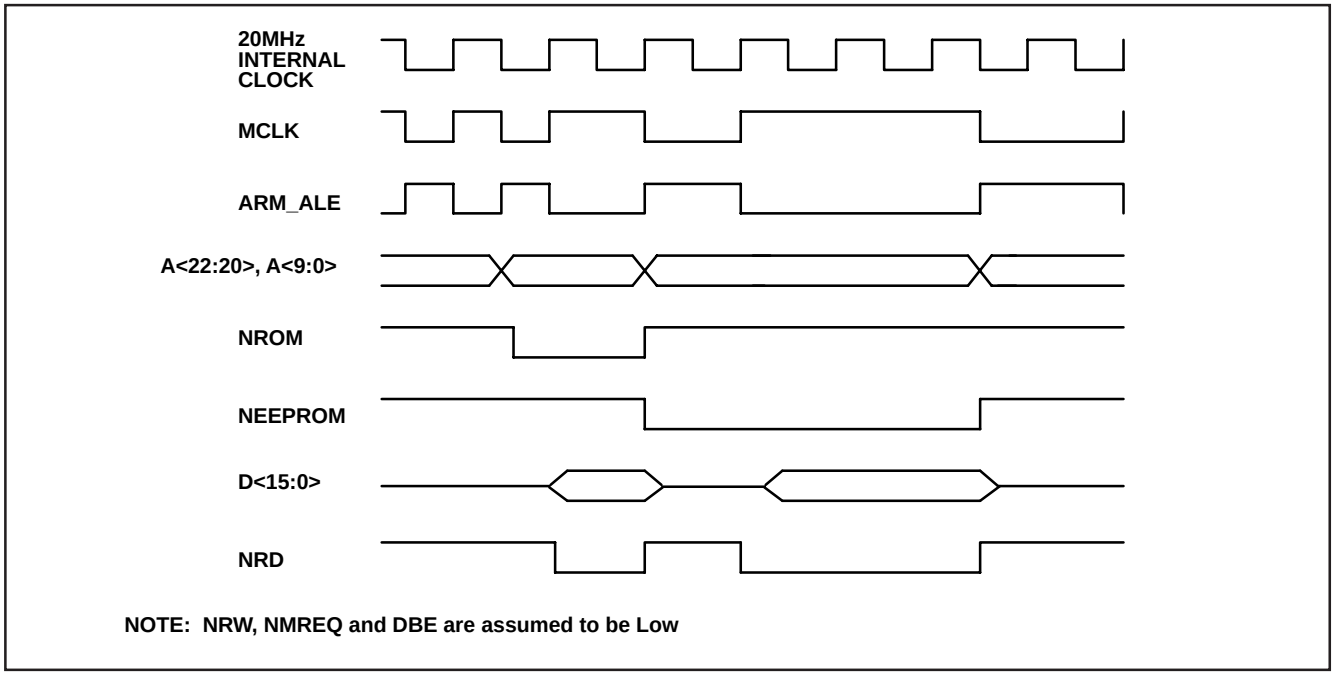


Fig.17 ROM (1 wait state) and EEPROM/spare (2+1wait states) Read Cycles

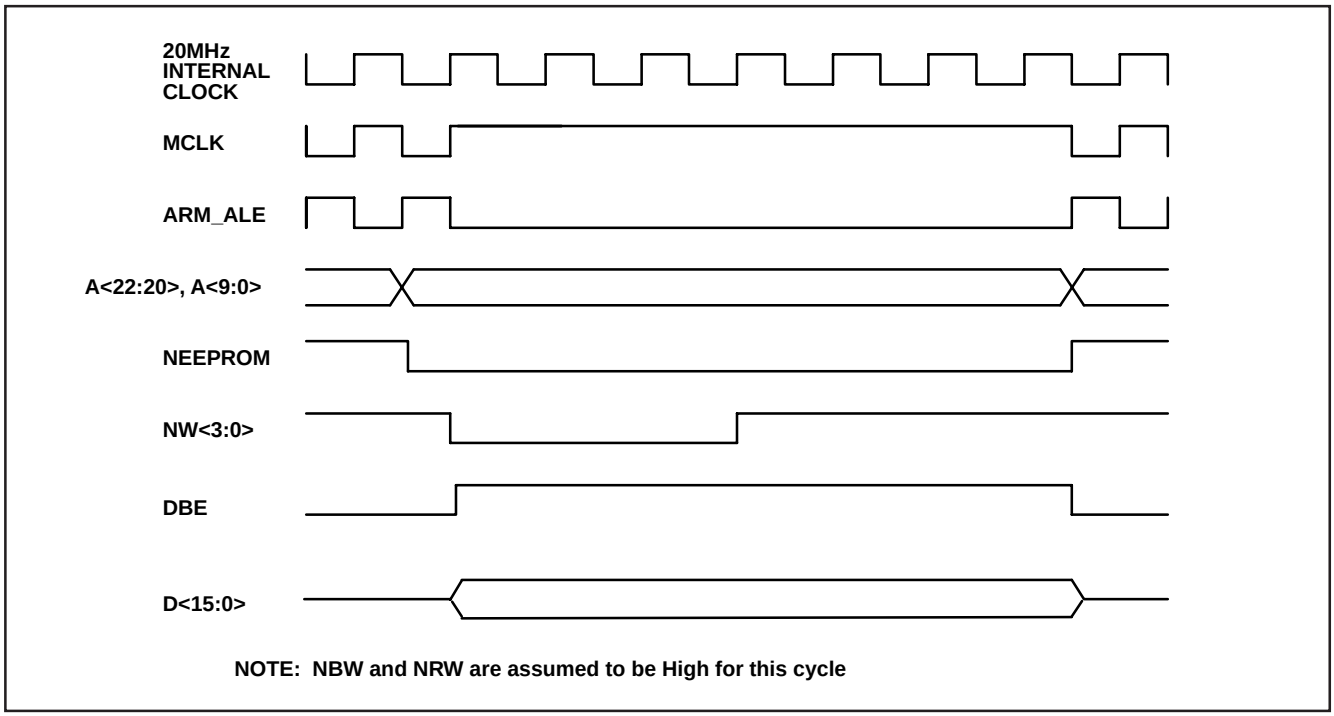


Fig.18 EEPROM (or Spare) Write Cycle

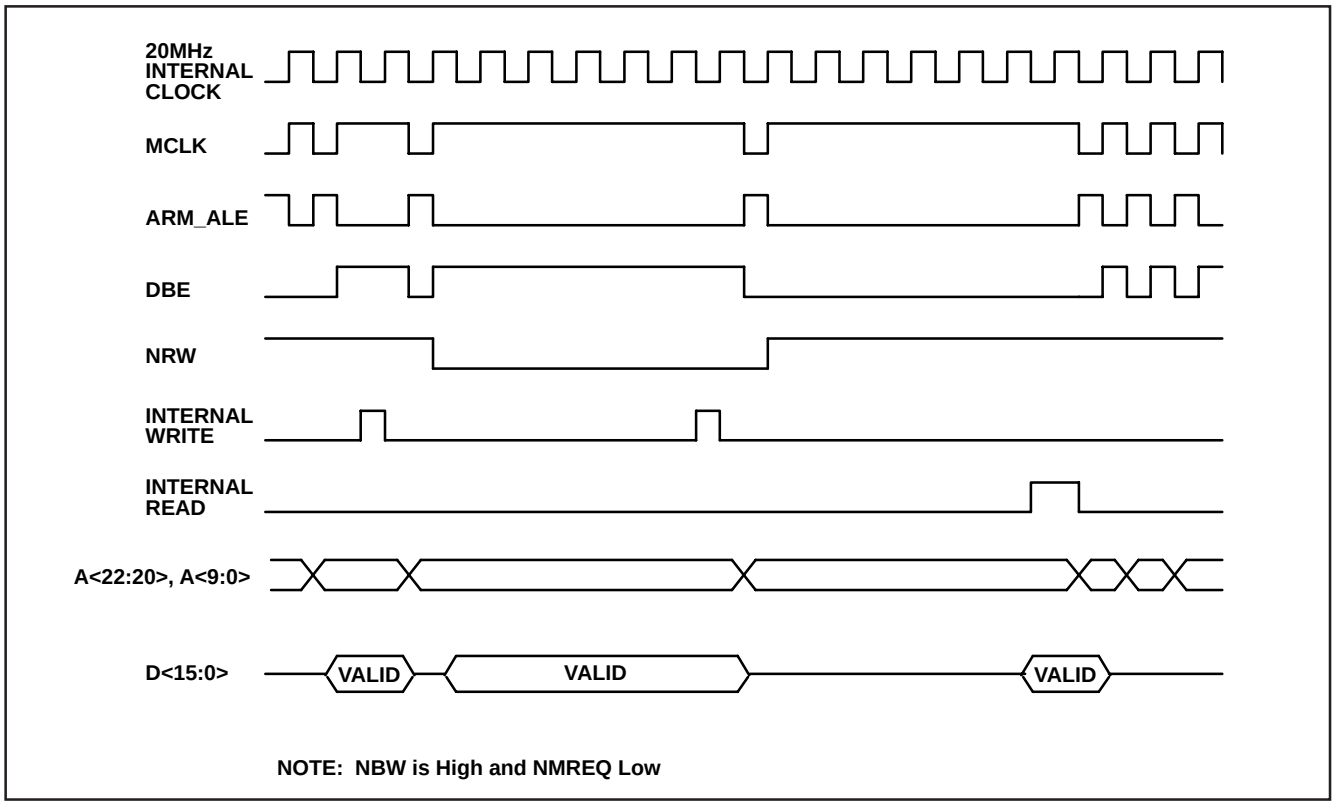


Fig.19 Correlator write and read cycles

Debug (Abort) Function

This is a feature designed to aid debugging and functions as follows:–

In ARM System Mode, the MULTI_FN_IO pin can be configured as a TRIGGER input to the Debug block via the IO_CONFIG register (see Detailed Description of Registers). In this mode a rising edge at the MULTI_FN_IO pin will generate a valid ARM data Abort sequence at the ABORT pin as shown in Fig. 20.

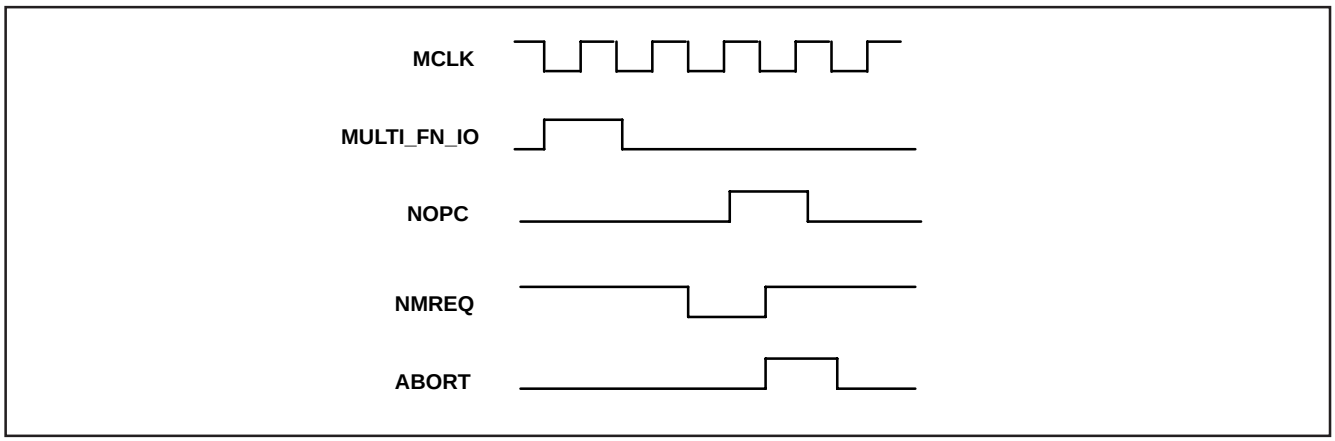


Fig.20 Debug (Abort) Function

Standard Interface Mode

This mode allows the GP2021 to be interfaced to most standard 16 and 32 bit microprocessors as shown in Fig. 21. No memory control is provided, so external glue logic may be required in order to interface the microprocessor to memory.

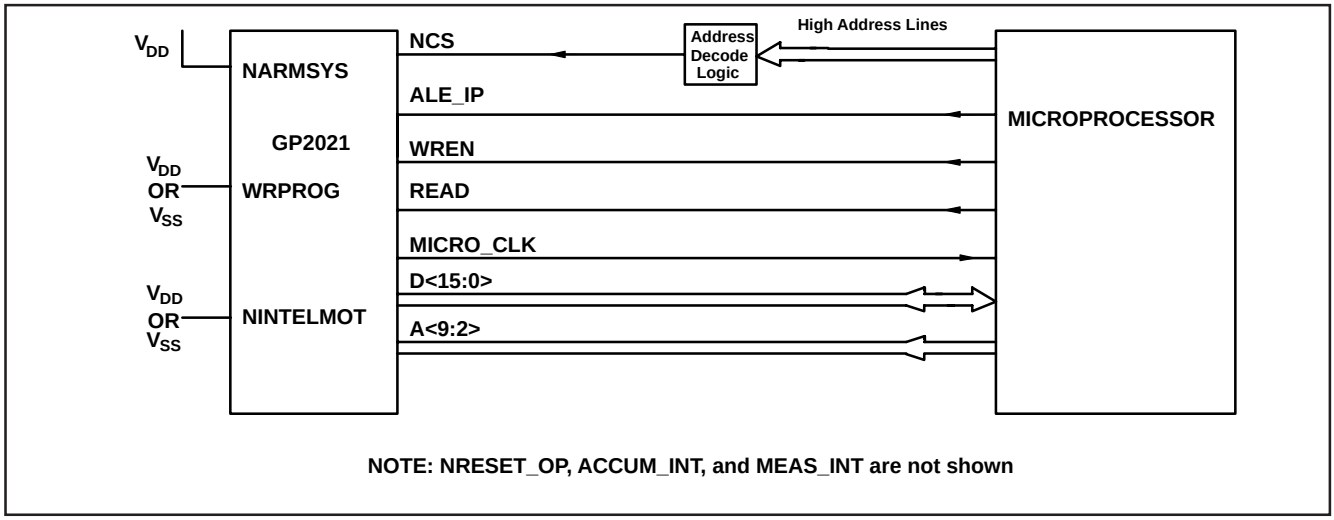


Fig.21 Standard Interface Mode

Control Signals

In Standard Interface Mode (NARMSYS held high), the microprocessor interface of the GP2021 consists of two mode control pins, (NINTELMOT and WRPROG), and the control signals themselves, (ALE_IP, NCS, WREN and READ; the exact function of which is dependent upon the interface style selected).

Motorola Style Interface

(NINTELMOT = '1', WRPROG = 'X')

The WRPROG mode control pin is not used in Motorola Interface mode and should be tied High or Low. The ALE_IP (Address Latch Enable input) pin is used to transparently latch the address lines A<9:2> to the GP2021. If these address lines are already latched externally, this pin may be tied High. Note that the internal ALE signal is inhibited during a read or write strobe so the address lines may be changed once the read or write strobe has become active. The WREN pin acts as a WRITE/READ ENABLE strobe (active High) with the READ pin selecting either a READ strobe (READ = '1') or a WRITE strobe (READ = '0'). In a similar way to the addresses being latched during a read or write strobe, the READ signal is also latched during a data strobe and may be changed towards the end of the cycle.

The NCS pin is an active low chip select used to gate out the internal read and write strobes. In Standard Interface Mode, the GP2021 can best be visualised in terms of 3 signals, ALE_INT, WRSTROBE_INT and RDSTROBE_INT, the internal ALE, write strobe and read strobe signals. In Motorola Style Interface Mode these signals are derived as follows:

ALE_INT=ALE_IP. $\overline{(\overline{WR}STROBE\_INT + RDSTROBE\_INT)}$
WRSTROBE_INT = $\overline{NCS}$.WREN.$\overline{READ}$
RDSTROBE_INT = $\overline{NCS}$.WREN.READ

INTEL 80186 Style Interface

(NINTELMOT = '0', WRPROG = '0')

In the 80186 Style Interface mode the ALE_IP acts as an Address Latch Enable input (as in Motorola mode), used to transparently latch the address lines A<9:2> to the GP2021. Similar to Motorola mode, if the addresses are latched externally this pin may be tied High. Whereas Motorola mode used a single strobe input and a Read/$\overline{Write}$ level to denote read and write strobes, both INTEL modes use a pair of strobe inputs, one for reads, and one for writes. In this mode, READ acts as the active low read strobe (READ =$\overline{RDSTROBE}$) and WREN the active low write strobe (WREN= $\overline{WRSTROBE}$). NCS is the active low chip select used to gate out internal data strobes.

ALE_INT=ALE_IP
WRSTROBE_INT = $\overline{NCS}$.$\overline{WREN}$
RDSTROBE_INT = $\overline{NCS}$.$\overline{READ}$

INTEL 486 Style Interface

(NINTELMOT = '0', WRPROG='1')

The Intel 486 Style Interface is similar to the 80186 style interface, with similar separate read and write strobes. Some of the later Intel microprocessors (notably the i486) have a very small delay between the rising edge of ALE and the falling edge of the read or write strobes. Due to the pre-charged nature of the data–out bus of the Correlator, the address inputs must remain stable throughout the read strobe, and the small delay from ALE to read strobe would produce insufficient address setup times for correct operation. The 486 style interface mode removes this problem by gating both the read and write strobes such that they are inhibited until the falling edge of ALE_IP. The ALE_IP pin must not be tied High in 486 Style Interface mode.

ALE_INT= ALE_IP
WRSTROBE_INT = $\overline{NCS}$. $\overline{WREN}$. $\overline{ALE\_IP}$
RDSTROBE_INT = $\overline{NCS}$. $\overline{READ}$. $\overline{ALE\_IP}$

Reset

The NRESET_IP pin allows the GP2021 to be provided with an external system reset.
For further information refer to System Reset in Standard Interface Mode.

Register Addressing

As shown in the GP2021 Register Map, register addresses differ from those in ARM System Mode. In particular in Standard Interface Mode the GP2021 address bus interface is via A<9:2>, with NCS acting as its chip select input. The address pins A0, A1 in ARM System Mode now become the NRESET_IP and ALE_IP inputs. Hence, depending upon the system configuration employed, A<9:2> of the GP2021 could be connected to the microprocessor address pins A<7:0>.

CONTROLLING THE GP2021

The following section describes typical methods for controlling the GP2021. These include: signal acquisition and tracking, carrier phase measurement and timemark generation.

Search Operation

To perform signal acquistion, the carrier frequency and code phase space needs to be searched until the signal is detected. The maximum carrier frequency excursion from its nominal value is defined by the maximum carrier Doppler shift plus the maximum receiver clock error. The maximum code phase is defined by the (fixed) code length. Typically, all code phases will be searched at a given carrier frequency before advancing to the next carrier frequency bin and repeating the code phase search.

Carrier DCO Programming

The following registers:
CHx_CARRIER_DCO_INCR_HIGH
(or X_DCO _INCR_HIGH),and
CHx_CARRIER_DCO_INCR_LOW are programmed in sequence with the relevant data according to the frequency bin being searched. It is always necessary to write to both the _HIGH and _LOW registers. Carrier DCO programming will become effective as soon as the channel is released (made active). If the channel is already active, writes to CHx_CARRIER_DCO_INCR_LOW are effective immediately. (A small delay of up to 175ns will occur, to allow synchronisation of the processor write operation to the chip operation.)

Code DCO Programming

The CHx_CODE_DCO_INCR_HIGH
(or X_DCO_INCR_HIGH)
and the CHx_CODE_DCO_INCR_LOW registers are programmed in sequence with the relevant data according to the estimated code frequency offset. It is always necessary to write to both _HIGH and _LOW registers. Code DCO programming will become effective as soon as the channel is released (made active). If the channel is already active, writes to CHx_CODE_DCO_INCR_LOW are effective immediately. (A small delay of up to 175ns will occur to allow synchronisation of the processor write operation to the chip operation).

Code Generator Programming

For each channel, the CHx_SATCNTL register is programmed as follows:

(i) Set the SOURCESEL bit to select the input signal source.
(ii) Set the TRACK_SEL bits to set the Tracking arm code to either early or late (with respect to the Prompt arm).
(iii) Set the G2_LOAD bits to select the required PRN code.
(iv) Program the CHx_CODE_SLEW register with the desired code phase offset. The slew operation will become effective upon CHx_RSTB release. The first DUMP will generate accumulated data for the channel and set the associated CHx_NEW_ACCUM_DATA status bit.
(v) Release the relevant CHx_RSTB bits of the RESET_CONTROL register to make the channel active.

When the code clock is inhibited (to slew the code phase) the Integrate and Dump module is held reset. It will start to accumulate correlation results only after the slew operation is completed.

A search for a satellite on more than one channel may be performed using the MULTI channel addresses and different code slew values as appropriate.

Reading the Accumulated Data

At each DUMP the corresponding CHx_NEW_ACCUM_DATA status bit is set in the ACCUM_STATUS_A register. The status register, together with all accumulation registers (CHx_I_TRACK, CHx_Q_TRACK, CHx_I_PROMPT, CHx_Q_PROMPT) are mapped into consecutive addresses. These can be read as a consecutive block, if required, after every ACCUM_INT interrupt. Alternatively, the Status Registers may be polled. The Accumulation registers are not overwrite protected, therefore the system must respond quickly when new data becomes available. Whether or not it is necessary to process the accumulation at every DUMP is dependent upon the application. The order of reading them is optional, but ideally the CHx_Q_PROMPT register should be read last, because this resets the CHx_NEW_ACCUM_DATA bit.

The CHx_MISSED_ACCUM bits in the ACCUM_STATUS_B register indicate that new accumulated data has been missed. These can only be cleared by a write to CHx_ACCUM_RESET or by deactivating the channel.

Search on Other Code Phases

When it is desired to correlate on the next code phase, such as one whole chip later, the CODE_SLEW has to be programmed with a value of 2 (the units are half code chips). The slew will occur on the next DUMP. The effect of CODE_SLEW is relative to the current code phase. To repeat a CODE_SLEW, the register needs to be written to again even if the same size slew is required.

Once the signal has been detected (correlation threshold exceeded), the code and carrier tracking loops can be closed. The tracking loop parameters must be tailored in the software to suit the application.

Data Bit Synchronisation

The data bit synchronisation algorithm should find the data bit transition instant. The processor calculates the present one millisecond epoch and programs this value into the 1MS_EPOCH counter. Ideally, epoch counter accesses should occur following the reading of the accumulation register at each DUMP.

Alternatively, the epoch counters can be left free–running and the offset can be added by the software each time it reads the epoch registers. Note that if the integration is performed across bit boundaries, the integration result can be very small.

Reading the Measurement Data

At each TIC, the measurement data is latched in the Measurement Data registers

(CHx_EPOCH,
CHx_CODE_PHASE,
CHx_CARRIER_DCO_PHASE,
CHx_CARRIER_CYCLE_HIGH,
CHx_CARRIER_CYCLE_LOW,
CHx_CODE_DCO_PHASE).

The ACCUM_STATUS_B or MEAS_STATUS_A register must be polled at a rate greater than the TIC rate (to see if a TIC has occurred), otherwise measurement data will be lost. The ACCUM_INT or MEAS_INT events can be used

to instigate this operation. The reading of measurement data can be either interrupt driven or polled. For the interrupt driven method the microprocessor reads the ACCUM_STATUS_B or MEAS_STATUS_A register after each MEAS_INT, and if the TIC bit is set, subsequently reads the Measurement data. For the polled method the ACCUM_STATUS_A register is always read following every ACCUM_INT. In addition the ACCUM_STATUS_B register is read on each ACCUM_INT to ensure no Accumulated Data has been missed and to check the TIC bit (along with several other status bits). The software tests the TIC bit to determine if new Measurement Data is available to be read.

Preset Mode

Each channel can be programmed into PRESET mode by writing a High into the PRESET/UPDATEB bit of the CHx_SATCNTL register.

When a TIC occurs, the satellite code, epoch value and slew numbers are loaded, and a new phase programmed into the Code DCO regardless of its previous value. Prior to the TIC the channel operates with its previous settings.

Preset Mode has no effect on the Carrier DCO and Carrier Cycle Counter.

If Preset mode is initiated, it should be allowed to operate to completion. The required sequence of operations is as follows:

(i) Write into CHx_SATCNTL to select the PRESET mode, together with the appropriate new settings.

ii) Load the Code and Carrier DCO increment values.

Note: These will take effect immediately thereby influencing the current measurements.

iii) Load the following Registers: CHx_CODE_DCO_PHASE, CHx_CODE_SLEW and CHx_EPOCH_COUNT_LOAD. It is important that the CHx_EPOCH_COUNT_LOAD occurs last, because it enables the preset operation on the next TIC.

Interrupts

There are 2 interrupt sources: ACCUM_INT and MEAS_INT. Their sense is dependant upon the selected microprocessor interface mode. The default ACCUM_INT period is 505.05µs. However, it can be reconfigured via the PROG_ACCUM_INT register or by changing the INTERRUPT_PERIOD or FRONT_END_MODE bits in the SYSTEM_SETUP register. The default MEAS_INT period is 50ms. However, this can be reconfigured via the PROG_TIC_HIGH and PROG_TIC_LOW registers.

Signal Path Delay
Introduced by Hardware Signal Processing

When it is desired to generate an accurate time reference from GPS signals or to time–stamp position fixes the delays in the receiver must be allowed for. The signal path delay has two components, an Analogue path delay which varies with temperature and component tolerances; and a Digital path delay which is constant if oscillator drift variations are neglected.

The Digital delay is easier to estimate and is made up of the following:

In Real_Input mode:

(i) The time from the sampling edge of the SIGN and MAG bits in the front end (SAMPCLK) to the re–sampling in the Sample Latch (175 ns less the propagation delay of SAMPCLK to the Front–end).

(ii) Plus the time for the correlation in the Correlator on these same SIGN and MAG bits (125 ns).

(iii) Plus the delay in the accumulator to latch the sampled data (175 ns).

(iv) Less the time between the correlation and the TIC clock phase which is before the accumulator latch phase (75 ns), Giving a total of 400 ns less the SAMPCLK delay.

In Complex_Input mode:

(i) The time for the correlation in the Correlator on the SIGN and MAG bits after sampling (114 ns).

(ii) Plus the delay in the accumulator to latch the sampled data (171 ns).

(iii) Less the time between the correlation and the TIC clock phase which is before the accumulator latch phase (86 ns), giving a total of 199 ns.

The Analog delay through the radio receiver is set by such parameters as group delay in filters, which for the bandwidths used for C/A code will be in the region of 1 to 2 ms and so swamps the digital delay, but this can be measured and corrected for.

Integrated Carrier Phase Measurement

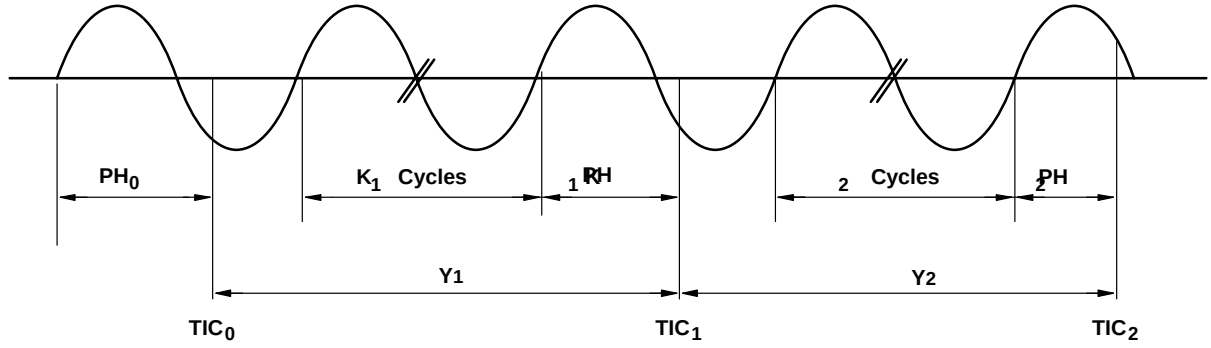
The Correlator tracking channel hardware allows measurement of integrated carrier phase through the CHx_CARRIER_CYCLE_HIGH and _LOW and the CHx_CARRIER_DCO_PHASE registers, which are part of the Measurement Data sampled at every TIC. The CHx_CARRIER_CYCLE_HIGH and _LOW registers contain the (20 bit) number of positive–going zero crossings of the Carrier DCO; this will be one more than the number of full cycles elapsed (4 bits are in _HIGH and 16 in _LOW register). The CHx_CARRIER_DCO_PHASE register contains the cycle fraction or phase, with 10 bit resolution to give $2\pi / 1024$ radian increments.

To get the Integrated Carrier Phase over several TIC periods all that is needed is to read the CHx_CARRIER_CYCLE_HIGH and _LOW registers at every TIC and sum the readings. This gives a number 1 higher than the number of complete carrier cycles, when a carrier cycle is measured from one positive–going zero crossing to the next.

To this number, the fractional carrier cycle at the end has to be added, and the fractional carrier cycle at the beginning has to be subtracted. Both numbers are read from the CHx_CARR_DCO_PHASE register. The total phase change can be calculated as follows :

Integrated Carrier Phase =
$2\pi * \sum$ Numbers in Carrier Cycle Counter
+ final Carrier DCO phase
–Initial Carrier DCO phase

Fig. 22 shows how this equation is derived.



1. reading at TIC_0 : $CHx\_CARR\_DCO\_PHASE_0 = PH_0$
2. reading at TIC_1 : $CHx\_CARR\_DCO\_PHASE_1 = PH_1$
   $CHx\_CARR\_CYCLE_1 = K_1 + 1$
3. reading at TIC_2 : $CHx\_CARR\_DCO\_PHASE_2 = PH_2$
   $CHx\_CARR\_CYCLE_2 = K_2 + 1$

$$\Delta Y1 = 2\pi * K_1 + (2\pi - PH_0) + PH_1$$
$$= 2\pi(K_1 + 1) - PH_0 + PH_1$$
$$= 2\pi * (CHx\_CARR\_CYCLE_1 - CHx\_CARR\_DCO\_PHASE_0 /1024 + CHx\_CARR\_DCO\_PHASE_1/1024)$$

$$\sum \Delta Y = 2\pi * (\sum_{i=1}^{last} CHx\_CARR\_CYCLE_i \quad CHx\_CARR\_DCO\_PHASE_0 \ 1024 \quad CHx\_CARR\_DCO\_PHASE_{last} \ 1024)$$

Note: The Carrier Cycle Counter value is stored at every TIC and the Counter is reset

Fig.22 Integrated carrier phase

This Integrated Carrier Phase may be related to the delta–range, (the change in distance to each satellite). When used with the orbital parameters of the satellites, the delta–ranges give a measure of the receiver's movement between fixes, which is independent of those fixes and so can be used to smooth them. It can also give a velocity directly. The delta–ranges will be noisy and most of the value is due to satellite movement so the determination of velocity must use data from adequately separated TICs. For position smoothing all delta–ranges may be included in the input to the navigation filter, as that filter will perform a running average of the delta–ranges as well as the ranges.

Timemark Generation

The GP2021 is capable of generating an accurate TIMEMARK timing output on one of the discrete outputs if required. TIMEMARK is intended to be a UTC aligned timing output with an accurate 1 second period and a pulse width of 1ms. The TIMEMARK output is always derived from a rising edge on TIC, and for UTC aligned operation the TIC counter must be brought into phase with UTC. This is done by modifying the division ratio of the TIC counter for a single TIC period, by increasing or reducing the division ratio, thus slewing the phase of TIC. Since the TIC counter is incremented every 175ns which is not an exact sub–multiple of 1 second it is also necessary to continually monitor the relationship between TIC and UTC to keep TIC in phase with UTC. Once TIC is in phase with UTC, the TIMEMARK output can be derived from TIC using one of 2 methods both of which involves writing to TIMEMARK_CONTROL: (1) The GP2021 can be armed to produce a TIMEMARK output at the next TIC only, or (2) It can be programmed to give a TIMEMARK output every n TICs starting at the next TIC.

A separate counter resets the TIMEMARK output giving a 1ms pulse width. The TIC counter can be programmed with an accuracy of 175ns in Real_Input mode or 171.4ns in Complex_Input mode. This determines the accuracy of the TIMEMARK output. If the TIC is continually synchronised to keep the rising edge as close as possible to UTC, the internal TIMEMARK will be within 100ns (4/7 x 175ns) of UTC in Real_Input mode or 85.7ns (3/6 x 171.4ns) of UTC in Complex_Input mode. In addition, there may be a delay of up to 50ns in getting the TIMEMARK output off chip, giving a maximum error of 150ns (Real_Input) or 135.7ns (Complex_Input) between TIMEMARK and UTC. It should be noted that due to the need to re–synchronise TIC, a jitter of up to 175ns may be present on TIMEMARK, along with any jitter and drift present on the input clock. The pulse width of TIMEMARK (in seconds) is either (5714 + 2/7) * (7/ Master Clock Frequency) for Real_Input mode giving 1.0000000ms (assuming an accurate 40MHz master clock input) or (5833 + 1/6) * (6 / Master Clock Frequency) for Complex_Input mode giving 0.9999714ms (assuming an accurate 35MHz master clock input).

DETAILED DESCRIPTION OF REGISTERS

GP2021 Register Map

The register map of the GP2021 is shown below. The addresses are complete, and it should be noted that all the register addresses are word–aligned, i.e. A0 and A1 are not used. Adjacent register addresses thus increment by 4, in ARM System Mode. However, in Standard Interface Mode, the GP2021 address lines A<9:2> could be connected to the processor address lines A<7:0>. Note that in this mode pins A0 and A1 are allocated other functions.

		ADDRESS (Hex)		ADDRESS (Hex)	REGISTERS
REGISTER BLOCK		ARM SYSTEM MODE A<22:20>	A,9:0>	STANDARD INTERFACE MODE A<9:2>	
CORRELATOR					
	CNTL	2	000 to 01C	00 to 07	CHo Control
	CNTL	2	020 to 03C	08 to OF	CH1 Control
	CNTL	2	040 to 05C	10 to 17	CH2 Control
	CNTL	2	060 to 07C	18 to 1F	CH3 Control
	CNTL	2	080 to 09C	20 to 27	CH4 Control
	CNTL	2	0A0 to 0BC	28 to 2F	CH5 Control
	CNTL	2	0C0 to 0DC	30 to 37	CH6 Control
	CNTL	2	0E0 to 0FC	38 to 3F	CH7 Control
	CNTL	2	100 to 11C	40 to 47	CH8 Control
	CNTL	2	120 to 13C	48 to 4F	CH9 Control
	CNTL	2	140 to 15C	50 to 57	CH10 Control
	CNTL	2	160 to 05C	58 to 5F	CH11 Control
	CNTL	2	180 to 19C	60 to 67	MULTI Control
		2	1A4	69	X_DCO_INCR_HIGH
		2	1AC	6B	PROG_ACCUM_INT
		2	1B4	6D	PROG_TIC_HIGH
		2	1BC	6F	PROG_TIC_LOW
	CNTL	2	1C0 to 1DC	70 to 77	ALL Control
		2	1EC	7B	TIMEMARK_CONTROL
		2	1FO	7C	TEST_CONTROL
		2	1F4	7D	MULTI_CHANNEL_SELECT
		2	1F8	7E	SYSTEM_SETUP
		2	1FC	7F	RESET_CONTROL
		2	200 to 20C	80 to 83	Status Registers
	ACCUM	2	210 to 21C	84 to 83	CHO Accumulate
	ACCUM	2	220 to 22C	88 to 8B	CH1 Accumulate
	ACCUM	2	230 to 23C	8C to 8F	CH2 Accumulate
	ACCUM	2	240 to 24C	90 to 93	CH3 Accumulate
	ACCUM	2	260 to 26C	98 to 9B	CH5 Accumulate
	ACCUM	2	270 to 27C	9C to 9F	CH6 Accumulate
	ACCUM	2	280 to 28C	A0 to A3	CH7 Accumulate
	ACCUM	2	290 to 29C	A4 to A7	CH8 Accumulate
	ACCUM	2	2A0 to 2AC	A8 to AB	CH9 Accumulate
	ACCUM	2	2B0 to 2BC	AC to AF	CH10 Accumulate
	ACCUM	2	2C0 to 2BC	B0 to B3	CH11 Accumulate
	ACCUM	2	2D0 to 2DC	B4 to B7	MULTI Accumulate
	ACCUM	2	2E0 to 2EC	B8 to BB	ALL Accumulate

REGISTER BLOCK	ADDRESS (Hex) ARM SYSTEM MODE A<22:20>	A,9:0>	ADDRESS (Hex) STANDARD INTERFACE MODE A<9:2>	REGISTERS
REAL -TIME CLOCK				
	3	000	C0	RTC_LS
	3	004	C1	RTC_2ND
	3	008	C2	RTC_MS
	3	00C	C3	CLOCK_RESET
	3	010	C4	WATCHDOG_RESET
DUART				
	3	040	D0	TX_DATA_A, RX_DATA_A
	3	044	D1	TX_DATA_A, RX_DATA_B
	3	048	D2	CONFIG_A, STATUS_A
	3	04C	D3	CONFIG_A, STATUS_B
	3	050	D4	CH10 Control
	3	054	D5	CH11 Control
	3	058	D6	MULTI Control
	3	05C	D7	X_DCO_INCR_HIGH
SYSTEM CONTROL				
	3	080	E0	WAIT_STATE
	3	084	E1	SYSTEM_CONFIG
	3	088	E2	Not Used
	3	08C	E3	SYSTEM_ERROR_STATUS
	3	090	E4	DATA_RETENT
GENERAL CONTROL				
	3	0C0	F0	IO_CONFIG
	3	0C4	F1	TEST_CONFIG
	3	0C8	F2	DATA BUS TEST

Table 8: GP2021 Register Map

Correlator Registers

Addresses for the Correlator Registers may be calculated from a base address with an increment for a particular register.

The base addresses for the CNTL and ACCUM register blocks for each channel in the Correlator are shown in the GP2021 Register Map, the increments being given below:

eg. CH3_CODE_DCO_INCR_LOW = 060H + 018H = 078H

Tracking Channel Registers

ADDRESS (Hex)		WRITE FUNCTION	READ FUNCTION
ARM MODE SYSTEM MODE	**STANDARD INTERFACE**		
CNTL + 00	CNTL + 0	SATCNTL	CODE_SLEW
+ 04	+ 1	CODE PHASE COUNTER*	CODE_PHASE
+ 08	+ 2	CARRIER_CYCLE_COUNTER*	CARRIER_CYCLE_LOW
+ 0C	+ 3	CARRIER_DCO_INCR_HIGH	CARRIER_DCO_PHASE
+ 10	+ 4	CARRIER_DCO_INCR_LOW	EPOCH (Latched0
+ 14	+ 5	CODE_DCO_INCR_HIGH	CODE_DCO_PHASE
+ 18	+ 6	CODE_DCO_INCR_LOW	CARRIER_CYCLE_HIGH
+ 1C	+ 7	EPOCH_COUNT_LOAD	EPOCH_CHECK (Not latched)
ACCUM + 00	ACCUM + 0	CODE_SLEW_COUNTER	I_TRACK
+ 04	+ 1	ACCUM_RESET	Q_TRACK
+ 08	+ 2	not used	I_PROMPT
+ 0C	+ 3	CODE_DCO_PRESET_PHASE	Q_PROMPT

NOTE: The registers labelled * (the CODE_PHASE_COUNTER and CARRIER_CYCLE_CONTROL) can only be written to if 'Test' mode has been selected by setting bit 3 of the TEST CONTROL register to High.

ADDRESS (Hex)		WRITE FUNCTION	READ FUNCTION
ARM SYSTEM MODE	**STANDARD INTERFACE MODE**		
200	80	STATUS	ACCUM_STATUS_C
204	81	not used	MEAS_STATUS_A
208	82	not used	ACCUM_STATUS_A
20C	83	not used	ACCUM_STATUS_B

In both the ACCUM and CNTL sections there are some addresses labelled ALL or MULTI in place of CHx. Writing to these addresses will write to all channels or to a selection set by MULTI_CHANNEL_SELECT in one operation and so may be used to initialise the system quickly or to load the next search settings with little bus use. This is a write only function and the corresponding CHx read functions are not available at addresses labelled ALL or MULTI.

It can be seen that the addresses in CNTL are used to control the device in write mode but give the Measurement Data when in read mode.

Apart from the Code and Carrier DCO increment values all data transfers are only 16 bit wide. Writes to the Code and Carrier DCO's are 32 bit data transfers where the _HIGH word should be written first and will be retained in the 16 to 32 bit interface until the _LOW word is written, which must occur as the next write to the chip. All 32 bits will then be transferred into the DCO increment register. Data is written to an input buffer in the 16 to 32 bit interface and will be transferred to its destination register during the next full cycle of the 7 (or 6) phase clock. Write cycles should therefore have a period of at least 300 ns. The X_DCO_INCR_HIGH may be used to write the high bits of the increment number to any or all DCO's as an alternative to using the CHx_CODE CARRIER_DCO_INCR– _HIGH addresses. By using this address, there is no need to wait 300ns before writing the _LOW part. For further information refer to General Interface Timing in Microprocessor Interface section.

The bit assignments for the Correlator registers are given below, but two write–only registers do not have any data bits, these are:

(1) A write to the CHx_ACCUM_RESET register (irrespective of what data is written) will reset the ACCUM_STATUS_A, ACCUM_STATUS_B, and ACCUM_STATUS_C registers for that channel.
(2) A write to the STATUS register (irrespective of what data is written) will latch the state of the various status flags into
ACCUM_STATUS_A,
ACCUM_STATUS_B,
ACCUM_STATUS_C
Registers for all channels. This allows a polling based rather than Interrupt driven tracking scheme.

The registers are listed in alphabetical order and not in address order to allow easy reference to each section. Unless otherwise stated the LSB is bit 0 and the MSB is bit 15 or as far up the register as there is data. Note that most registers do not have both read and write functions, and many addresses are shared between read–only and write–only registers having different functions.

ACCUM_STATUS_A
(Read Address)

Bit	Bit Name
15	ACCUM_INT
14	Not used –LOW
13	Not used –LOW
12	Not used –LOW
11	CH11_NEW_ACCUM_DATA
10	CH10_NEW_ACCUM_DATA
9	CH9_NEW_ACCUM_DATA
8	CH8_NEW_ACCUM_DATA
7	CH7_NEW_ACCUM_DATA
6	CH6_NEW_ACCUM_DATA
5	CH5_NEW_ACCUM_DATA
4	CH4_NEW_ACCUM_DATA
3	CH3_NEW_ACCUM_DATA
2	CH2_NEW_ACCUM_DATA
1	CH1_NEW_ACCUM_DATA
0	CH0_NEW_ACCUM_DATA

ACCUM_STATUS_A is a register containing the state of twelve status bits sampled and latched on the active edge of every ACCUM_INT. They can also be sampled and latched on request, by performing a write operation to STATUS. (This is safe only if the interrupts are stopped, by setting INTERRUPT_ENABLE bit to LOW in the SYSTEM_SETUP register.) The microprocessor must respond to each ACCUM_INT and read the channel registers before the next DUMP is due in that channel.

The ACCUM_INT bit is set HIGH at every ACCUM_INT and is reset by reading the ACCUM_STATUS_A register. This status bit is reset by a hardware master reset but not by a software reset (MRB).

The CHx_NEW_ACCUM_DATA status bit indicates that a DUMP has occurred in that channel, and that new Accumulated Data is available to be read.

Each bit is cleared by the trailing edge of a read of the associated CHx_Q_PROMPT register or by a write to CHx_ACCUM_RESET.

Note that the channel specific bits of this register will not show their new value until after an active edge of ACCUM_INT or a write to the STATUS register. Disabling a channel will however, clear the bit immediately.

ACCUM_STATUS_B
(Read Address)

Bit	**Bit Name**
15	DISCIP_GLITCH
14	DISCIP
13	TIC
12	MEAS_INT
11	CH11_MISSED_ACCUM
10	CH10_MISSED_ACCUM
9	CH9_MISSED_ACCUM
8	CH8_MISSED_ACCUM
7	CH7_MISSED_ACCUM
6	CH6_MISSED_ACCUM
5	CH5_MISSED_ACCUM
4	CH4_MISSED_ACCUM
3	CH3_MISSED_ACCUM
2	CH2_MISSED_ACCUM
1	CH1_MISSED_ACCUM
0	CH0_MISSED_ACCUM

The lower 12 bits of ACCUM_STATUS_B bits are sampled and latched on the active edge of every ACCUM_INT signal. They can be sampled and latched on request by performing a write operation to STATUS (as with ACCUM_STATUS_A).

The DISCIP_GLITCH bit will be set High if a glitch to Low has occurred on the DISCIP pin since the last read of this register. It is cleared by reading this ACCUM_STATUS_B register. This bit is reset by a hardware master reset (RESETB at Low) but not by a software reset. The minimum reliably detectable glitch width is 25ns.

The DISCIP bit indicates the level on the DISCIP input pin at the time this read occurs and may be used to interface a hardware condition (such as a ready flag from a UART or the PLL LOCK signal from a front–end) to the microprocessor without using an interrupt. This bit is not reset by a hardware master reset nor by an MRB.

The TIC bit is set High at every TIC and is cleared by reading this ACCUM_STATUS_B register. Its purpose is to tell the microprocessor that new Measurement Data is available. It is reset by a hardware master reset (RESETB at Low) but not by an MRB in RESET_CONTROL.

Provided that interrupts are enabled, the MEAS_INT bit is set High at each TIC and 50 ms before each TIC (if the TIC period is greater then 50 ms), and is cleared by reading this register. This bit can be used as a flag to the microprocessor, to time software module swapping. It is reset by a hardware master reset (RESETB at Low), but not by a software reset. CHx_MISSED_ACCUM status bit indicates (when High) that there has been missed Accumulated Data due to a new DUMP in CHx before the previous data has been read. This bit is latched until the associated CHx_ACCUM_RESET is written to. If any data is missed due to the reading process being too slow this must be allowed for in the software, such as by checking the Navigation Message data bit transitions independently of the sets of Accumulated Data reads. If too much data is lost the system signal to noise ratio will be degraded. The primary purpose of these bits is as a check on how well the tracking routines are working – once the whole design is complete these bits should not become set.

Note that the channel specific bits of this register will not show their new value until after an active edge of ACCUM_INT or a write to the STATUS register. Disabling a channel will however, clear the bit immediately.

ACCUM_STATUS_C
(Read Address)

Bit	**Bit Name**
15	not used – LOW
14	not used – LOW
13	not used – LOW
12	not used – LOW
11	CH11_EARLY_LATEB
10	CH10_EARLY_LATEB
9	CH9_EARLY_LATEB
8	CH8_EARLY_LATEB
7	CH7_EARLY_LATEB
6	CH6_EARLY_LATEB
5	CH5_EARLY_LATEB
4	CH4_EARLY_LATEB
3	CH3_EARLY_LATEB
2	CH2_EARLY_LATEB
1	CH1_EARLY_LATEB
0	CH0_EARLY_LATEB

ACCUM_STATUS_C bits are sampled and latched on the active edge of every ACCUM_INT signal, or they can be sampled and latched on request by performing a write operation to STATUS (as with ACCUM_STATUS_A).

CHx_EARLY_LATEB status bit indicates the code type for the Accumulated Data on the Tracking arm of channel CHx when that channel is in Dithering mode. A High indicates an EARLY code and a Low indicates a LATE code. Each individual bit is determined on the DUMP that sets CHx_NEW_ACCUM_DATA to High for that channel. In other modes the bit is of no use.

Note that the channel specific bits of this register will not show their new value until after an active edge of ACCUM_INT or a write to the STATUS register. Disabling a channel will however, clear the bit immediately.

CHx_ACCUM_RESET
(Write Address)

Bits 15 to 0: Not used.

These are write–only locations provided to allow resetting of the status bits ACCUM_STATUS_A, ACCUM_STATUS_B, and ACCUM_STATUS_C associated with a given channel or all channels. When these locations are written to, the data is irrelevant.

CHx_CARRIER_CYCLE_COUNTER,
MULTI_CARRIER_CYCLE_COUNTER,
ALL _CARRIER_CYCLE_COUNTER
(Write Address)

A write to these registers only has effect when in test mode (bit 3 of TEST_CONTROL set High). The value on the bus is loaded into the lower 16 bits of the CHx_CARRIER_CYCLE_COUNTER along with zeros into the upper 4 bits.

CHx_CARRIER_CYCLE_HIGH,
CHx_CARRIER_CYCLE_LOW
(Read Address)

_HIGH bits 15 to 4 : not used – LOW when read.
_HIGH bits 3 to 0: Carrier Cycle Count bits 19 to 16.
_LOW bits 15 to 0: Carrier Cycle Count bits 15 to 0.

The Correlator tracking channel hardware allows for measurement of integrated carrier phase through the CHx_CARRIER_CYCLE_HIGH and _LOW and the CHx_CARRIER_DCO_PHASE registers, which are part of the Measurement Data sampled at every TIC. The CHx_CARRIER_CYCLE_HIGH and _LOW registers contain the 20 bit number of positive going zero crossings of the Carrier DCO (4 bits are in _HIGH and 16 in _LOW). The cycle fraction can be read from the CHx_Carrier_DCO_Phase register.

In the CHx_CARRIER_CYCLE counter, a TIC generates two consecutive actions. First it latches the 4 more significant bits of the cycle counter into CHx_CARRIER_CYCLE_HIGH and the 16 less significant bits into CHx_CARRIER_CYCLE_LOW. Then it resets the cycle counter.

After each TIC, every time the Carrier DCO accumulator generates an overflow as a result of a carrier cycle being completed, the cycle counter increments by one.

In Real_Input mode the nominal CARRIER DCO frequency with no Doppler and no oscillator drift compensation is 1·405396825 MHz, so in 100 ms, there will be about 140540 cycles.

In almost all applications the number of Carrier DCO cycles does not vary much from one TIC interval to another so it is possible to predict the Most Significant Bits of the value, and then only read the CHx_CARRIER_CYCLE_LOW register.

CHx_CARRIER_CYCLE_HIGH and _LOW contents are not protected by an overwrite protection mechanism and so must be read before the next TIC.
For further information on the Carrier Cycle Counter refer to Detailed Operation of GP2021.*

* Refer to page 9.

CHx_CARRIER_DCO_INCR_HIGH,
X_DCO_INCR_HIGH,
MULTI_CARRIER_DCO_INCR_HIGH,
ALL_CARRIER_DCO_INCR_HIGH,
CHx_CARRIER_DCO_INCR_LOW,
MULTI_CARRIER_DCO_INCR_LOW,
ALL_CARRIER_DCO_INCR_LOW
(Write Address)

_INCR_HIGH bits 15 to 10: Not used in this operation.
_INCR_HIGH bits 9 to 0 : More significant bits (25 to 16) of the Carrier DCO phase increment when used before a write to _CARRIER_DCO_INCR_LOW.
_INCR_LOW bits 15 to 0 : Less significant bits (15 to 0) of the Carrier DCO phase increment.

The contents of registers _INCR_HIGH and_INCR_LOW are combined to form the 26 bits of the CHx_CARRIER_DCO_INCR register, the carrier DCO phase increment number. In order to write successfully, the top 10 bits must be written first, to any of the _HIGH addresses. They will be stored in a buffer and only be transferred into the increment register of the DCO together with the _LOW word. A 26 bit increment number is adequate for a 27 bit accumulator DCO, as the increment to the MSB is always zero.

The LSB of the INCR register represents a step given by:

Min Step Frequency	= (40MHz/7)/2 27
(in Real_Input mode)	= 42.57475mHz
Min Step Frequency	= (35MHz/6)/2 27
(in Complex_Input mode)	= 43.46172mHz
The output Frequency	= CHx_CARRIER_DCO_INCR * Min Step Frequency.

With a GP2015/GP2010 style front end, the nominal value of the IF is 1.405396826 MHz before allowing for Doppler shift or crystal error. Writing 01F7B1B9H into the CHx_CARRIER_DCO_INCR register will generate a local oscillator frequency of 1.405396845 MHz.

CHx_CARRIER_DCO_PHASE
(Read Address)

Bits 15 to 10: Not used – Low when read.
Bits 9 to 0: More significant bits (26 to 17) of CHx_CARRIER_DCO_PHASE as sampled at the last TIC. The weight of the least significant bit is 2 π / 1024 radians of a Carrier DCO cycle. These bits form an unsigned integer valid from 0 to 1023. CHx_CARRIER_DCO_PHASE provides

sub-cycle phase measurement information and so complements the information given by CHx_CARRIER_CYCLE_HIGH and _LOW.

The register value is latched on each TIC and is not protected by any overwrite protection mechanism.

CHx_CODE_DCO_INCR_HIGH,
X_DCO_INCR_HIGH,
MULTI_CODE_DCO_INCR_HIGH,
ALL_CODE_DCO_INCR_HIGH,
CHx_CODE_DCO_INCR_LOW,
MULTI_CODE_DCO_INCR_LOW,
ALL_CODE_DCO_INCR_LOW
(Write Address)

_INCR_HIGH bits 15 to 9: Not used in this operation. _INCR_HIGH bits 8 to 0: More significant bits (24 to 16) of the Code DCO phase increment when used before a CODE_DCO_INCR_LOW.

_INCR_LOW bits 15 to 0: Less significant bits (15 to 0) of the Code DCO phase increment.

The contents of registers _INCR_HIGH and _INCR_LOW are combined to form the 25 bits of the CHx_CODE_DCO_INCR register, the Code DCO phase increment number. In order to write successfully, the top 9 bits must be written first, to any of the _HIGH addresses. They will be stored in a buffer and only be transferred into the increment register of the DCO together with the _LOW word. A 25 bit increment number is adequate for a 26 bit accumulator DCO as the increment to the MSB is always zero.

The LSB of the INCR register represents a step given by:

Min Step Frequency	= (40MHz/7)/2 ^{26}
(in Real_Input mode)	= 85.14949mHz
Min Step Frequency	= (35MHz/6)/2 ^{26}
(in Complex_Input mode)	= 86.92344mHz
The output Frequency	= CHx_CODE_DCO_INCR * Min Step Frequency.

Note: The Code DCO drives the Code Generator to give half chip time steps and so must be programmed to twice the required chip rate. This means that the chip rate resolution is 42·57475mHz in Real_Input mode or 43.46172mHz in Complex_mode.

The nominal frequency is 1.023000000 MHz before allowing for Doppler shift or crystal error. Writing 016EA4A8H into the CHx_CODE_DCO_INCR register will generate a chip rate of 1.022999968 MHz in Real_Input mode. In Complex_mode, 01672922H will generate a chip rate of 1.022999970 MHz.

CHx_CODE_DCO_PHASE
(Read Address)

Bits 15 to 10: Not used, (Low when read).

Bits 9 to 0: CHx_CODE_DCO_PHASE: Contains the ten more significant bits (25 to 16) of the Code DCO phase accumulator sampled at a TIC event. It is an unsigned integer valid from 0 to 1023. The weight of the least significant bit is 2 π /1024 radians, 2 π being half of a code chip, so the pseudorange resolution is 1/2048 of a chip, (equivalent to 0·15 metre or 0·5ns).

The CHx_CODE_DCO_PHASE content is not protected by any overwrite protection mechanism.

CHx_CODE_DCO_PRESET_PHASE,
MULTI_CODE_DCO_PRESET_PHASE,
ALL_CODE_DCO_PRESET_PHASE
(Write Address)

Bits 15 to 8: Not used.

Bits 7 to 0: More significant bits (25 to 18) of the Code DCO phase which is to be loaded at the next TIC event in PRESET mode.

In PRESET mode, the 8 bits of the CHx_CODE_DCO_PRESET_PHASE register, with zeros filling the lower bits, are transferred to the CODE DCO accumulator on the next TIC. The previous accumulator phase is totally overwritten. The PRESET_PHASE register is a write–only register and it can be written to at any time in PRESET mode or in UPDATE mode, but only has effect when PRESET mode is entered. The weight of the least significant bit of PRESET phase is 2 / 256 radians of a half chip cycle.

In UPDATE mode this register has no use other than as preparation for PRESET mode.

Refer to Detailed Operation of GP2021 for further information on PRESET mode. *

* Refer to page 9.

CHx_CODE_PHASE
(Read Address)
CHx_CODE_PHASE_COUNTER,
MULTI_CODE_PHASE_COUNTER,
ALL_CODE_PHASE_COUNTER
(Write Address)

Bits 15 to 11: Not used, Low when read.

Bits 10 to 0: CHx_CODE_PHASE (Read) – This is the state of the Code Phase Counter, (an 11–bit binary up counter clocked by the Code Generator Clock), stored on TIC. The phase is expressed as a number of half code chips and ranges from 0 to 2046 half chips. A reading of 2046 is very rare and can only occur if the TIC captures the Code phase just after the counter reaches 2046 and before it is reset by a DUMP from the C/A Code Generator. DUMP also increments the Epoch counter, so the meaning of a phase value of 2046 + the previous Epoch value is the same as a phase value of 0 + the incremented Epoch value, and either is valid. If a TIC occurs during a Code Slew the reading will be 0, and that channel's Measurement Data is of no use.

Bits 10 to 0: (Write) loads the 11 bits of the CHx_CODE_PHASE_COUNTER. A write to these registers is only possible in test mode, enabled by setting the TM_TEST (bit of TEST_CONTROL) to High.

CHx_CODE_SLEW
(Read Address)
CHx_CODE_SLEW_COUNTER,
MULTI_CODE_SLEW_COUNTER,
ALL_CODE_SLEW_COUNTER
(Write Address)

Bits 15 to 11: Not used.

Bits 10 to 0 : An unsigned integer ranging from 0 to 2047 representing the number of code half chips to be slewed immediately after the next DUMP if in UPDATE mode or after the next TIC, if in PRESET mode. Since there are only 2046

half chips in a GPS C/A code, a programmed value of 2047 is equivalent to a programmed value of 1, but the next DUMP event will take place 1 ms later. In PRESET mode, the slew timing is set only by TIC, which will also reset the code generator, (no DUMP is needed). A non–zero slew must always be programmed when using PRESET mode.
The CHx_CODE_SLEW register can be written to at any time. If two accesses have taken place before a DUMP in UPDATE mode or before a TIC when in PRESET mode, the latest value will be used at the next slew operation. During the time a slew process is being executed, any further write access to the CHx_CODE_SLEW register will be stored until the following DUMP and then cause the transfer of this new value into the counter. This situation may be avoided by synchronising the access with the associated CHx_NEW_ACCUM_DATA status bit.

If a channel is inactive, a non–zero slew value should be written into CHx_CODE_SLEW before the channel is released. This write will be acted on immediately the reset is released.

If a TIC occurs during or soon after a slew the channel will not be locked to the satellite, so the Measurement Data for that channel will not be of use.

The ability to read the Slew counter is included only for testing hardware or software and has no other use. It will only give a non–zero result if the read occurs during the actual slew operation. An example of a slewing event is shown in Fig.23.

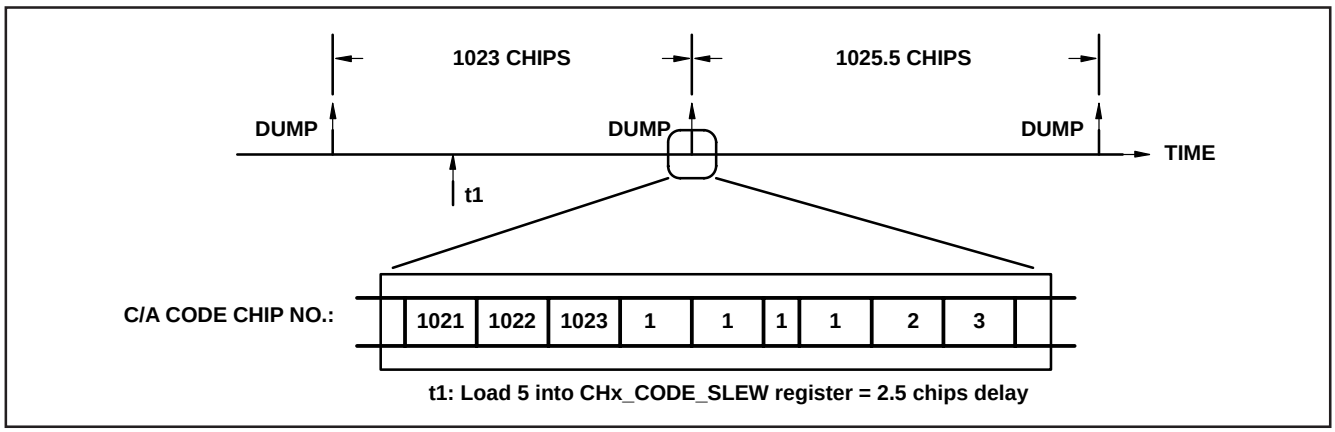


Fig.23 Slew timing in UPDATE mode

CHx_EPOCH_CHECK
(Read Address)
Bits 15 to 14: Not used.
Bits 13 to 8 : Instantaneous value of CHx_20MS_EPOCH.
Bits 7 to 5 : Not used.
Bits 4 to 0 : Instantaneous value of CHx_1MS_EPOCH.

Reading this address gives the instantaneous value of the CHx_1MS_EPOCH and the CHx_20MS_EPOCH counters. It can be used to verify if the Epoch counters have been properly initialised by the software. Its value is not latched and is incremented on each DUMP. To ensure the correct result, this register should be read only when there is no possibility of getting a DUMP during the read cycle, by synchronising the read to NEW_ACCUM_DATA. The ranges of these values are the same as those seen in the CHx_EPOCH register.

CHx_EPOCH
(Read Address)
Bits 15, 14, 7, 6 and 5: Not used. Read gives Low.
Bits 13 to 8: CHx_20MS_EPOCH: The 20 ms epoch counter value that was sampled at the last TIC event, with a valid range from 0 to 49.
Bits 4 to 0: CHx_1MS_EPOCH: The 1 ms epoch counter value that was sampled at the last TIC event, with a valid range from 0 to 19.

CHx_EPOCH_COUNT_LOAD
MULTI_EPOCH_COUNT_LOAD
ALL_EPOCH_COUNT_LOAD
(Write Address)
Bits 15, 14, 7, 6, and 5: Not used.
Bits 13 to 8: CHx_20MS_EPOCH: The value to be loaded into the 20 millisecond epoch counter, with a valid range from 0 to 49.
Bits 4 to 0: CHx_1MS_EPOCH: The value to be loaded into the 1 millisecond epoch counter, with a valid range from 0 to 19. This operation is affected by the current channel mode, (PRESET or UPDATE). In UPDATE mode, the data written into these registers is immediately transferred to the 1 ms and 20 ms epoch counters. In PRESET mode however, the data is transferred only after the next TIC. It is important to load the CHx_EPOCH register last in the PRESET mode loading sequence because the trailing edge of a write to this register enables the whole PRESET operation on the next TIC. Refer to Detailed Operation of the GP2021 for more details of the PRESET mode. *

* Refer to page 23

CHx_I_TRACK,
CHx_Q_TRACK,
CHx_I_PROMPT,
CHx_Q_PROMPT
(Read Address)

Bits 15 to 0: Accumulated Data registers, which are used on each DUMP to store the 16–bit Integrate–and–Dump accumulator results. The values contained in the registers are 2's complement values with the valid range of the data from -2^{15} to $+(2^{15}-1)$.

These registers are read–only registers which can be read at any time. Their content is not protected by any overwrite protection mechanism, so the set of four registers must be read soon after a ACCUM_INT to be sure that newer data will not cause an overwrite part way through the set. The CHx_I_PROMPT and CHx_Q_PROMPT contain the Accumulated Data from the Prompt arm. The CHx_I_TRACK and CHx_Q_TRACK contain the Accumulated Data from the Tracking arm.

To track satellites correctly, only data read with the CHx_NEW_ACCUM_DATA bit set High should be used. An overflow or underflow condition cannot be reached.

CHx_SATCNTL,
MULTI_ SATCNTL,
ALL_SATCNTL
(Write Address)

Bit	Bit Name
15	GPS_NGLON
14 to 13	TRACK_SEL
12	PRESET/UPDATEB
11	CODE_OFF/ONB
10	SOURCESEL
9 to 0	G2_LOAD (9 to 0)

CHx_SATCNTL is a write–only register that can be written into at any time. Any modification to the content is effective at the next DUMP in UPDATE mode or at the next TIC in PRESET mode for all bits, apart from PRESET UPDATEB,which defines whether a channel is in PRESET or UPDATE mode. It is important to program this register first when starting the initialisation of a PRESET sequence to get the channel into PRESET mode, or the other write operations will act too soon.

G2_LOAD (9 to 0), bits 9 to 0: C/A CODE SELECTION FUNCTION: The CHx_SATCNTL register programs the CODE GENERATOR by setting the G2 register to the appropriate starting pattern to generate the required GPS or INMARSAT–GIC codes. The G2_LOAD register may be programmed at any time but the value is only used when the code sequence restarts, at the following DUMP in UPDATE mode, or at the following TIC in PRESET mode. The pattern to load is the register state for the time of the second code chip. The following table shows the values required to select one of the 37 GPS or the 8 INMARSAT–GIC possible PRN (Pseudo Random Noise) patterns.

In UPDATE mode, the C/A code generated by the CODE GENERATOR will be changed at the DUMP following the write to CHx_SATCNTL and at this DUMP the Accumulated Data will be valid for the previous code selection. Later DUMPs will be valid for the new code.

If all zeros are loaded into the G2 register it will not clock out, and the G1 generator code will be seen on the output. This is an illegal state which is only of use for chip testing.

GPS PRN Signal No	BIT SETTING 9 to 0	GPS PRN Signal No	BIT SETTING 9 to 0
1	3F6H	24	338H
2	3ECH	25	27OH
3	3D8H	26	OEDH
4	3BOH	27	1COH
5	04BH	28	38OH
6	096H	29	22BH
7	2CBH	30	056H
8	196H	31	OACH
9	32CH	32	158H
10	3BAH	33	2BOH
11	374H	34*	058H
12	1DOH	35	18BH
13	3AOH	36	316H
14	340H	37*	058H
15	280H	201 GIC	2C4H
16	100H1	202 GIC	10AH
17	113H	205 GIC	3E3H
18	226H	206 GIC	OF8H
19	04CH	207 GIC	25FH
20	098H	208 GIC	1E7H
21	130H	209 GIC	2B5H
22	260H	211 GIC	10EH
23	267H		

Table 9 : G2 LOAD settings required for satellite selection.

*C/A Codes 34 and 37 are equivalent.
Notes: PRN sequences 33 to 37 are reserved for non–satellite uses (e.g. ground transmitters).

PRN sequences 201 to 211 are selected for INMARSAT GIC (GPS Integrity Channel) use.Due to the initialisation of the Early–Prompt–Late shift register, all codes will always start with a "1" for the first bit of the sequence after a Code change or a Code Slew. Subsequent cycles of the PRN sequence will be correct for the chosen satellite.

SOURCESEL, bit 10: Selects which input source to be used by the channel when in Real_Input mode. Low selects SIGN0 and MAG0, High selects SIGN1 and MAG1.

CODE_OFF/ONB, bit 11: When Low, the code is output normally, but when High, the Prompt, Early and Late codes are held High (code mixer outputs exactly follow inputs) and the Early–minus–late code is held LOW. This is intended for test purposes only.

PRESET/UPDATEB, bit 12: When High sets the channel into Preset mode, or when Low, sets the channel into Update mode. This bit is cleared to Low after the Preset function has been done, that is after the first TIC following the loading of the Epoch counters.

TRACK_SEL (1 and 0), bits 14 and 13: Select the appropriate code to be produced by the Tracking arm output of the code generator as follows:

14	13	CODE SELECT
0	0	Early code
0	1	Late code
1	0	Dithering code (alternating early and late)
1	1	Early–minus–late code

Table 10: TRACK_SEL bit settings for Tracking arm code selection.

When the dithering code has been selected, the Tracking arm will use the EARLY code for 20 periods of the Gold code, the LATE code for the next 20 periods and then this process of alternating between Early and Late code will be repeated indefinitely. The Tracking Arm will toggle between Early or Late Codes on every increment of a 20ms Epoch Count. Its state can be determined by reading the ACCUM_STATUS_C register.

The output code is a sequence of +1's and –1's for all code types except EARLY–MINUS–LATE where the result can also be a 0. In EARLY–MINUS–LATE mode the values are not the +2,0, –2 that results from the calculation (+1 or –1) – (+1 or –1), but are halved to +1, 0, –1. This must be considered when choosing thresholds in the software as the correlation results will be exactly half of the values otherwise expected.

GPS NGLON, bit 15: Setting this bit to Low changes the C/A code generator mode to GLONASS mode, to generate the fixed 511 bit sequence used by all GLONASS Satellites. After a master reset, GPS mode is selected, but with all zeros in the G2 generator, the G1 code is seen at the output of the C/A code generator.

MEAS_STATUS_A
(Read Address)

Bit	Bit Name
15 to 14	Not Used
13	TIC
12	MEAS_INT
11	CH11_MISSED_MEAS_DATA
10	CH10_MISSED_MEAS_DATA
9	CH9_MISSED_MEAS_DATA
8	CH8_MISSED_MEAS_DATA
7	CH7_MISSED_MEAS_DATA
6	CH6_MISSED_MEAS_DATA
5	CH5_MISSED_MEAS_DATA
4	CH4_MISSED_MEAS_DATA
3	CH3_MISSED_MEAS_DATA
2	CH2_MISSED_MEAS_DATA
1	CH1_MISSED_MEAS_DATA
0	CH0_MISSED_MEAS_DATA

When a CHx_MISSED_MEAS_DATA status bit is High, it indicates that one or more sets of measurement data have been missed since the last read from this register. It is set High by a read from the Code Phase Counter of the same channel, when the previous value in the Code Phase Counter has not been read, and is reset by a read from the MEAS_STATUS_A register or by disabling the channel.

If this register is always read after the Code Phase Counter, it indicates whether measurement data has been missed before the last read of the Code Phase Counter. All CHx_MISSED_MEAS_DATA bits are set Low by a hardware or software reset.

The MEAS_INT bit is set High at each TIC and 50 ms before each TIC (if TIC period is greater then 50 ms), and is cleared by reading this register. The purpose of the bit, is a flag to the microprocessor, to time software module swapping. This bit is reset by a hardware master reset (RESETB at Low) but not by a software reset.

The TIC bit is set High at every TIC and is cleared by reading this register. The purpose of the bit is to tell the microprocessor that new Measurement Data is available. This bit is reset by a hardware master reset (RESETB at Low) but not by an MRB in RESET_CONTROL.

MULTI_CHANNEL_SELECT
(Write Address)

Bit	Bit Name
15 to 12	Not Used
11	CH11_SELECT
10	CH10_SELECT
9	CH9_SELECT
8	CH8_SELECT
7	CH7_SELECT
6	CH6_SELECT
5	CH5_SELECT
4	CH4_SELECT
3	CH3_SELECT
2	CH2_SELECT
1	CH1_SELECT
0	CH0_SELECT

CHx_SELECT, when set High, enables the Multi–channel write operations on CHx. This may be used to set several channels to mostly the same conditions. For a parallel search for one satellite, operations such as setting each Carrier DCO to the same frequency; or during that search, to adjust all selected channels by the same value, (such as a Code Slew to shift the code phases together to a new search area) could use this feature.

All CHx_SELECT are set Low by a (hardware or software) master reset.

PROG_ACCUM_INT
(Write Address)

Bits 15 to 13: Not Used.

Bits 12 to 0: ACCUM_INT Division Ratio.

The PROG_ACCUM_INT register location operates in conjunction with the INTERRUPT_PERIOD bit of the SYSTEM_SETUP register to set the period of the ACCUM_INT output. ACCUM_INT is generated by a 13 bit binary down counter which counts down to zero, producing an ACCUM_INT output. It then loads to a preset value stored in its preset register and starts to count down again. If the preset value is P, the count sequence is P, P–1, P–2, ..., 1, 0, P, P–1. Hence, the counter divides by P+1, producing an output with a period of (P+1) * clock period. Since the ACCUM_INT counter is clocked by the multi–phase clock, the clock rate is either 7 * clock period (nominally 40MHz, i.e. 25ns) for Real_Input mode, or 6 * clock period (nominally 35MHz, i.e.

28.571429ns) for Complex_Input mode. The value stored in the preset register can be modified in one of two ways: Either by toggling the INTERRUPT_PERIOD or FRONT_END_MODE bits of the SYSTEM_SETUP register, or by writing to the PROG_ACCUM_INT location. Either of these actions will overwrite the previous contents of the preset value and either one or both methods may be used. If the Interrupt Counter detects an edge on either the INTERRUPT_PERIOD or FRONT_END_MODE bits it will load one of four values in to the preset register, depending upon the new value of both INTERRUPT_PERIOD and FRONT_END_MODE. These four presets are as shown in Table 12.

The value for INTERRUPT_PERIOD = Low and FRONT_END_MODE = Low is also that loaded on a Master Reset. Alternatively the ACCUM_INT counter may be loaded by writing direct to the PROG_ACCUM_INT location. In this case the new ACCUM_INT period is as follows:

ACCUM_INT Period = (PROG_ACCUM_INT + 1) * 7 (40MHZ) (Real Input mode)

ACCUM_INT Period = (PROG_ACCUM_INT + 1) * 6 (35MHz) (Complex Input mode)

FRONT_END_MODE (In SYSTEM_SETUP)	INTERRUPT_PERIOD (in SYSTEM_SETUP)	Preset	ACCUM_INT Period
Low (Real_Input mode)	Low	0x0B45	(2885+1)* (7/40MHz) = 505.0500µs
Low (Real_Input mode)	High	0x1313	(4883+1)* (7/40MHz) = 854.70000µs
High (Complex_Input mode)	Low	0x0B81	(2945+1)* (6/35MHz) = 505.02857µs
High (Complex_Input mode)	High	0x1379	(4985+1)* (6/35MHz) = 854.74286µs

Table 12: ACCUM_INT Period settings

PROG_TIC_HIGH,
PROG_TIC_LOW
(Write Address)

PROG_TIC_HIGH Bits 4 to 0: More significant 5 bits of the TIC counter division ratio when programmed before a PROG_TIC_LOW.

PROG_TIC_LOW Bits 15 to 0: Least significant 16 bits of the TIC counter division ratio.

The PROG_TIC_HIGH and PROG_TIC_LOW register locations operate in conjunction with the FRONT_END_MODE bit of the SYSTEM_SETUP register to set the period of TIC. TIC is generated by a 21 bit binary down counter when it reaches zero. It then loads to a preset value stored in its preset register and starts to count down again. If the preset value is P, the count sequence is P, P–1, P–2, ..., 1, 0, P, P–1. Hence, the counter divides by P+1 producing an output with a period of (P+1) * clock period. Since the TIC counter is clocked by the multi–phase clock, the clock period is either 7 * clock period (nominally 40MHz i.e. 25ns) for Real_Input mode or 6 * clock period (nominally 35MHz i.e. 28.571429ns) for Complex_Input mode. The value stored in the preset register can be modified in one of two ways: Either by toggling the FRONT_END_MODE bit of the SYSTEM_SETUP register, switching into Complex_Input mode, or by writing to the PROG_TIC_HIGH/_LOW locations. Either of these actions will overwrite the previous contents of the preset value. If the TIC Counter detects an edge on the FRONT_END_MODE bit it will load one of two values into the preset register, depending upon its new value. These two presets are as shown in Table 13.

The value for FRONT_END_MODE = Low is also that loaded on a Master Reset. Alternatively, the TIC counter may be loaded by writing directly to the PROG_TIC locations. This may be achieved in one of two ways: Either the PROG_TIC_HIGH value can be written, followed by the PROG_TIC_LOW value, (at which point the full 21 bits are transferred to the preset register), or just the PROG_TIC_LOW value may be written to modify the lower 16 bits of the preset value. It should be noted that in the former case, the top 5 bits programmed as PROG_TIC_HIGH are stored locally to the TIC counter and even if a write to PROG_TIC_LOW does not directly follow the write to PROG_TIC_HIGH, the next PROG_TIC_LOW write will still transfer all 21 bits. It is also necessary to ensure that the write to PROG_TIC_HIGH precedes the write to PROG_TIC_LOW, rather than follows it. One further point to note is that the transfer of data to the TIC counter data latches occurs under control of the multi–phase clock write cycle and the write to the preset register happens subsequent to the main internal write. To ensure correct operation, a write to SYSTEM_SETUP, toggling the FRONT_END_MODE bit should not be directly preceded or followed by a write to PROG_TIC_LOW. In addition to the 300ns delay normally required between write cycles, a further 100ns delay is required between these two types of writes. A write to SYSTEM_SETUP toggling the FRONT_END_MODE bit followed directly by a PROG_TIC_HIGH / PROG_TIC_LOW sequence is permissible, since the write to PROG_TIC_HIGH does not instigate a change of the preset register contents within the TIC counter.

Using the PROG_TIC write locations the TIC period is as follows:

TIC Period (Real_Input) = ((PROG_TIC_HIGH * 65536) + PROG_TIC_LOW+1)*7/(40MHZ)

TIC Period (Complex_Input) = ((PROG_TIC_HIGH * 65536) + PROG_TIC_LOW+1) * 6/(35MHZ)

FRONT_END_MODE (In SYSTEM_SETUP)	Preset Loaded	TIC Period
Low (Real_Input mode)	0x08B823	(2885+1)* (7/40MHz) = 505.0500µs
High (Complex_Input mode)	0x08E6A4	(4985+1)* (6/35MHz) = 854.74286µs

Table 13: TIC period setting

RESET_CONTROL

(Write Address)

Bit	Bit Name
15	Not used.
14	Not used.
13	Not used.
12	CH11_RSTB
11	CH10_RSTB
10	CH9_RSTB
9	CH8_RSTB
8	CH7_RSTB
7	CH6_RSTB
6	CH5_RSTB
5	CH4_RSTB
4	CH3_RSTB
3	CH2_RSTB
2	CH1_RSTB
1	CH0_RSTB
0	MRB, Active LOW software master reset

MRB: When Low (a software reset), the effect is similar to a hardware reset except that the clock generator, the time base generators, measurement data and peripheral functions are not affected and the Status bits ACCUM_INT, DISCIP, DISCIP_GLITCH, MEAS_INT, and TIC are not reset. MRB should be set to High to allow access to all of the various registers. MRB is set High by a hardware reset.

CHx_RSTB: When set active Low, the reset bit inhibits propagation of the clock phases to the CHx tracking channel and resets the Accumulated Data flags, Code DCO and Carrier DCO accumulators, the I & D accumulators, and the Code Phase Counter. A CHx_RSTB does not reset the Carrier Cycle, Code Slew or the Epoch counters. At the end of the reset, the channel enable resets the code generator to a previously programmed start phase. This is all required for the parallel search algorithm of one satellite signal using many channels in order to start from a known relative code phase on all the channels. All of the control registers in CHx can be programmed and read as usual during the reset state. To restart normal operation in several different channels at the same time, the corresponding CHx_RSTB bits should be set to High during the same write operation. All CHx_RSTB are set Low by a master reset, (both hardware and software), so a write Low to bit 0 of this register will force a Low onto bits 12 to 1 irrespective of what was on the bus.

Power consumption can be kept to a minimum by setting CHx_RSTB Low when a channel is not required.

STATUS

(Write Address)

Bits 15 to 0: not used

A write operation to this location, irrespective of the data on the bus, latches the state of all status bits contained in ACCUM_STATUS_A, ACCUM_STATUS_B, and ACCUM_STATUS_C registers. Performing a write to STATUS prior to reading the status registers ensures reading of stable status values. The latch takes effect within 300 ns of the trailing edge of the write pulse. The active edge transition of the ACCUM_INT signal will also latch the state of the status bits, thus it is not necessary to write to STATUS when the status registers are to be read as a response to the ACCUM_INT signal in an interrupt handling routine. The write to STATUS is required only when the status registers are read at times that are not synchronised to the interrupts. These two mechanisms are mutually exclusive and should not be used together – if both are used, a write to STATUS soon after the occurrence of an ACCUM_INT signal can result in confused readings. To avoid conflict the INTERRUPT_ENABLE in the SYSTEM_SETUP register should be set to Low if writes to STATUS are to be used.

If the INTERRUPT_ENABLE bit in SYSTEM_SETUP register is set to Low, the interrupt will not latch the status bits in the status registers, but a STATUS write access will do so.

SYSTEM_SETUP

(Write Address)

Bit	Bit Name
15 to 11	Not used
10	MEAS_INT_SOURCE
9	OPS_DRIVE_SEL
8	IPS_3V_MODE
7	INTERRUPT_PERIOD
6	FRONT_END_MODE
5	INTERRUPT_ENABLE
4	DISCOP_SELECT_100KHZ
3	DISCOP_SELECT_TIMEMARK
2	DISCOP_SELECT_CH0_DUMP
1	DISCOP
0	CARRIER_MIX_DISABLE

MEAS_INT_SOURCE: When set High the MEAS_INT output is cleared by a read of MEAS_STATUS_A, when Low by a read of ACCUM_STATUS_B. A master reset forces the MEAS_INT_SOURCE bit Low.

OPS_DRIVE_SEL: When set High this control bit increases the size of the output driver on ACCUM_INT, MEAS_INT, and D(15:0) pins so as to increase the drive of these pins if they are driving a large load. Master reset forces OPS_DRIVE_SEL to Low.

IPS_3V_MODE: When set High this control bit sets the input buffers on SIGN0, MAG0, SIGN1, and MAG1 for signals centred on mid–supply, for use with a Front–end running from a 3V supply. When Low, sets the thresholds to TTL levels, for 5V operation. Master reset forces IPS_3V to Low.

INTERRUPT_PERIOD: When Low, the approximate interrupt period is set to 505 s and when High it is set to 854 s. For more detail see the description of PROG_ACCUM_INT. Master reset forces INTERRUPT_PERIOD bit to Low.

FRONT_END_MODE: Selects either Real_Input mode when Low or Complex_Input mode when High. Master reset forces FRONT_END_MODE to Low.

INTERRUPT_ENABLE: When set Low the effect of the ACCUM_INT and MEAS_INT interrupts are disabled (masked) and when set High both are enabled. Master reset forces INTERRUPT_ENABLE to Low.

Bits 4 to 1 The signal provided on the DISCOP pin can be selected according to Table 14.

Bit				Signal On DISCOP output
4	**3**	**2**	**1**	
0	0	0	0	0 (Reset condition)
0	0	0	1	1
0	1	0	X	Timemark
0	X	1	X	Ch0 DUMP
1	X	X	X	100kHz Square wave

Table 10: TRACK_SEL bit settings for Tracking arm code selection.

CARRIER_MIX_DISABLE: When High the Carrier mixers are all driven by a fixed '+1' level on the Carrier DCO input port, so that the input data is passed unaltered to the Code mixer. Master reset forces the CARRIER_MIX_DISABLE bit to Low.

TEST_CONTROL
(Write Address)

Bit	Bit Name
15 to 12	Not Used
11 to 9	PATH_SEL<2:0>
8	EN_SCANPATH
7	Not Used
6	TEST_CACODES
5	TEST_DATA
4	TEST_SOURCE
3	TM_TEST
2	FE_TEST
1	EN_DUMMYTICS
0	EN_DUMMYDUMP

This register is purely to enable various test modes. A Master Reset will set all bits to Low, giving normal operation.

EN_DUMMYDUMP: When High, this bit changes the function of the NOPC/NINTELMOT input pin to be a DUMMYDUMP input, and if in Standard Interface Mode it also forces the microprocessor mode to Motorola. A DUMMYDUMP will operate in the same way as a normal DUMP (reset all of the code generators and transfer the contents of all integrators into the Accumulated Data registers). Each Low to High transition of NOPC/NINTELMOT will cause a DUMMYDUMP and if NOPC/NINTELMOT is already High when EN_DUMMYDUMP is set, one will also occur immediately. Selecting Dummy dump mode does not inhibit normal DUMP events. The NOPC/NINTELMOT pin must be held High for at least 200 ns for each DUMMYDUMP.

EN_DUMMYTICS: When High this bit changes the function of the DISCIP input pin to a DUMMYTIC input. This replaces the TIC from the timebase generator so that a TIC effect will only occur when there is a Low to High transition on DISCIP, to latch new Measurement Data. The DISCIP pin must be held High for at least 200 ns for each DUMMYTIC.

FE_TEST: When High this test control forces the SIGN input to channel 11 and the MAG input to channel 5 both to Low. This allows the evaluation of the front_end SIGN (on channel 5) and MAG (on channel 11) duty cycles. The Front end to be tested is selected by the SOURCESEL bits in CH5_SATCNTL and CH11_SATCNTL.

To get the SIGN and MAG count correctly into the accumulators, both the carrier and code mixers must be made transparent.

The carrier mixing may be disabled by either: (1) Setting CARRIER_MIX_DISABLE (bit 0 in SYSTEM_SETUP) to High to force a +1 on the Carrier DCO inputs to all channels or, (2) If continued position finding is required from the other channels during the test, by setting CH5_ and CH11_CARRIER_DCO_INCR to all 0's, to give a constant level (zero frequency). This level should be set to a known value by putting channels 5 and 11 briefly into the reset state (by using RESET_CONTROL register bits 6 and 12) during the time their Carrier DCO's are programmed to zero frequency. This reset forces the phase to all 0's and hence the drives to the Prompt In–phase mixer to a fixed +1 and not a randomly selected –2, –1, +1, or +2 that would result from just setting the frequency.

The C/A code mixing must be disabled by setting CODE_OFF/ONB (bits 11 in both CH5_ and CH11_SATCNTL) to High. However, as the period of the count is set by the DUMPs from the Code Generator, the DCO clock to the Code Generator must be set to the required frequency by programming the Code DCO even though the code output is disabled. A typical value is the frequency for the nominal code chipping rate, so that the SIGN and MAG counts are over a millisecond.

The results of monitoring the Front–end of the receiver may be used for fault diagnosis and also for tuning the parameters in the software for optimum satellite tracking with the particular Front–end or SIGN/MAG duty cycle.

To find the duty cycle of the SIGN signal, channel 5 is used. The In–phase accumulator CH5_I_PROMPT will add +1 for each SIGN sample at High and will add –1 for each SIGN sample at Low, so if the duty cycle is correct at 50%, the sum will always be close to zero and only differ by the imbalance of sampling at the beginning and end of the integration period.
The duty cycle may be calculated as follows:

N = Total No of samples in integration period.
N_{SIGN1} = Total No of samples for which SIGN was High.
N_{SIGN0} = Total No of samples for which SIGN was Low.
ACC5 = Total value in the CH5_I_PROMPT accumulator, as read after a DUMP.

$N = N_{SIGN1} + N_{SIGN0}$,
$ACC5 = N_{SIGN1} – N_{SIGN0}$
SIGN duty cycle = $R_S = N_{SIGN1} / N = (N + ACC5) / 2N$ (nominally 0.50)

To find the duty cycle of the MAG signal, channel 11 is used. The In–phase accumulator CH11_I_PROMPT will add –3 for each MAG sample at High and will add –1 for each MAG sample at Low. If the duty cycle is correct (30%), the sum will be: –1.6 * (Number of samples) plus an allowance for the imbalance of sampling at the beginning and end of the integration period. The duty cycle may be calculated as follows:

N = Total No of samples in integration period.
N_{MAG3} = Total No of samples for which MAG was High
N_{MAG1} = Total number of samples for which MAG was Low
ACC11 = Total value in the CH11_I_PROMPT accumulator, as read after a DUMP.
$N = N_{MAG3} + N_{MAG1}$,
$ACC11 = -3 * N_{MAG3} - N_{MAG1}$

MAG duty cycle, $Rm = Nmag3 / N = -(N + ACC11) / 2N$ (nominally 0·30).

TM_TEST: When High this bit puts all the Tracking Modules into a test mode, where it is possible to write to all CHx_CARRIER_CYCLE_COUNTERs and all CHx_CODE_PHASE_COUNTERs.

TEST_SOURCE: When High this bit enables a self–test generator formed from the CH0 Code Generator. The data replaces the SIGN0 and MAG0 inputs. It has a chip rate and phase set by the CH0_CODE_DCO and a carrier frequency set by the CH0_CARRIER_DCO. The code is set by writing the appropriate start value into the CH0_SATCNTL register, and the CH0_SLEW_COUNTER can be programmed to delay the start of the code generation by a number of half code chips. The three most significant bits of the Carrier DCO are decoded to give the SIGN with 50% of Highs and the MAG with 25% of Highs. The sign of the data pattern is set by TEST_DATA, EXORed with the CH0 C/A code.

TEST_DATA: This bit sets the sign of the modulation of the test data generated when TEST_SOURCE is set.

TEST_CACODES: When High, the inverted PROMPT codes for all channels, 0 to 11, are available for output on data bus bits 0 to 11 and can be seen in parallel by a read to any CH6 to CH11 read address.

EN_SCANPATH: When High the chip is in scan test mode, whereby:

DISCIP 1	becomes	SCAN_IN
DISCOP	becomes	SCAN_OUT
MULTI_FN_IO	becomes	SCANCLK
NOPC/NINTELMOT	becomes	SCANSEL

It should be noted that the DISCOP = SCAN_OUT function may be over–ridden by the DISCOP_SELECT_100KHZ function of SYSTEM_SETUP. It should also be noted that for correct operation the MULTI_FN_IO pin should be configured as a Discrete or Scan Clock Input via the IO_CONFIG register.

PATH_SEL<2:0>: To allow for simple factory testing of the chip, the GP2021 contains six separate scan paths, one for each of the major counters in the chip. Only one of these paths may be enabled at any time and the scan path to be used is selected via the PATH_SEL<2:0> bits as follows:

PATH_SEL<2:0>	Scan Path Selected
000	RTC Counters
001	ACCUM_INT Counter
010	TIC Counter
011	100KHz Output Counter
100	Timemark Pulse Width Counter
101	PLL_LOCK Filter Counter
11X	Not Used

TIMEMARK_CONTROL
(Write Address)

Bit	Bit name
15 to 7	not used
6 to 2	FREE_RUN_RATIO
1	FREE_RUN_TIMEMARK
0	ARM_TIMEMARK

The TIMEMARK Generator operates in one of two ways, either in armed mode, (not related to ARM System Mode) or in free run mode. In armed mode setting the ARM_TIMEMARK bit arms the TIMEMARK generator which subsequently produces a TIMEMARK output pulse coincident with the next rising edge of TIC. This then resets the ARM_TIMEMARK bit ready for a new arming sequence in the future. Alternatively, the TIMEMARK generator can be used in free–run mode, by setting the FREE_RUN_TIMEMARK bit High. This disables the ARM_TIMEMARK bit. In free run mode a TIMEMARK pulse is produced coincident with the first rising edge of TIC after the FREE_RUN_TIMEMARK bit has been set, and then on an integer number of TIC's determined by the FREE_RUN_RATIO bits. In free run mode the TIMEMARK period is:

TIMEMARK Period = (FREE_RUN_RATIO + 1) * TIC Period (Free run mode)

All the bits of TIMEMARK_CONTROL are cleared to Low by a Master Reset.

X_DCO_INCR_HIGH
(Write Address)

This register may be used to write the high bits for any Carrier or Code DCO in any channel. A write to X_DCO_INCR_HIGH must always be followed by a write to the appropriate CHx_CARRIER_DCO_INCR_LOW or CHx_CODE_DCO_INCR_LOW to define the destination and to complete the action.

Using X_DCO_INCR_HIGH rather than CHx_CARRIER_DCO_INCR_HIGH gives a quicker way of loading the whole DCO's values because the _LOW write may follow the X_DCO_INCR HIGH write immediately (without incurring a 300ns wait).

PERIPHERAL FUNCTIONS REGISTERS

The addresses for the Peripheral Functions Registers are shown in the GP2021 Register Map.

These registers may be either 8 or 16 bits wide. Registers which are byte wide are accessed via the top 8 bits of the data bus, D<15:8>. During a byte wide read D<7:0> are held Low.

Each of the registers for the Real Time Clock, Dual UART, System and General Control functions are described below.

Real Time Clock and Watchdog

The registers in the Real Time Clock are all byte wide.

RTC_LS, RTC_2ND, RTC_MS , (Read Addresses)

The clock time is output in these three eight bit read only registers. All three registers are latched when a read is performed of the LS Byte Register, so this should be read first. In Power Down Mode the clock continues to run but access to these registers is not possible.

CLOCK RESET

(Write Address)

A write to this address resets the clock divider and counter, regardless of the data word written.

WATCHDOG RESET

(Write Address)

A write to this address resets the watchdog timer, regardless of the data word written.

DUART

All the registers within the DUART are byte wide.

CONFIG_A, CONFIG_B (Write Address)

These registers allow the UARTs to be configured for receive baud rate, parity and loopback. The configuration bit functions are shown in Table 15. The missing binary combinations of bit settings should not be used as the results would be indeterminate.

Note that all bits are set Low by a UART A/B or a System reset, thus causing UART A/B to default to a receive baud rate of 300, no parity and no loopback.

Bit Setting					Function
Bit	11	10	9	8	Receiver Baud Rate
	0	0	0	0	300
	0	0	0	1	600
	0	0	1	0	1200
	0	0	1	1	2400
	0	1	0	0	4800
	0	1	0	1	9600
	0	1	1	0	19.2k
	0	1	1	1	38.4k
	1	0	0	0	76.8k
Bit	13	12			Parity
	0	0			No parity–bit not set or checked for
	1	1			Odd parity–parity added so that the toatl number of '1's in the word is even
	1	0			Even parity–parity added so that the total number of '1's in the word is even
Bit	14				Loopback
	0				No loopback–normal operation
	1				Loopback–the Tx output drives the Rx input and Tx pin is held HIGH
Bit	15				Test mode
	0				Test mode bit in Ch A only used for chip testing only. This bit must be set Low for Normal operation
	1				Test mode

Table 15: Configuration of UARTs through CONFIG_A and CONFIG_B registers.

STATUS_A, STATUS_B (Read Address)

Reading from these register addresses will give the current value of the channels status bits. The Status bit functions are as shown in Table 16.

Bit	SET (High) by	CLEARER (Low) by	RESET to
8	RX Valid Data Available	No RX Data	Low
9	RX FIFO Full	RX FIFO Not Full	Low
10	RX FIFO Overflow	Read of UART Status Register	Low
11	TX Transmitting	TX Register Empty	Low
12	TX FIFO Full	TX FIFO Not Full	Low
13	Parity Error Occured	Read of UART Status Register	Low Low
14	Framing Error	Read of Uart Status	Low
15	Not Used (Held High)		

Table 16: Status bits available when reading the STATUS_A and STATUS_B registers.

RESET_A,
RESET_B
(Write Address)

Writing to this register will reset the UART A/B, regardless of the data word written.

TX_DATA_A,
TX_DATA_B,
RX_DATA_A,
RX_DATA_B
(Write / Read Address)

These are Read/Write addresses to UARTs A and B, which allow bytes to be written to the TX FIFOs or received from the RX FIFOs.

TX_RATE_A,
TX_RATE_B
(Write Address)

These are write registers for UARTs A and B which allow the Transmit baud rates to be set as shown in Table 17. The missing binary combinations of bit settings should not be used as the results would be indeterminate.

Bit 11	10	9	8	Receiver Baud Rate
0	0	0	0	300
0	0	0	1	600
0	0	1	0	1200
0	0	1	1	2400
0	1	0	0	4800
0	1	0	1	9600
0	1	1	0	19.2k
0	1	1	1	38.4k
1	0	0	0	76.8k

Table 17: Transmit baud rate settings in the TX_RATE_A and TX_RATE_B registers.

Bits 12 to 15 are not used and may be set High or Low. Note that bits 8 to 11 are set Low by a UART A/B or System reset, thus causing the Transmitter to default to a baud rate of 300.

System Control

WAIT_STATE
(Write / Read Address)

This is a Read/Write register (8 bits wide), which allows the ROM (Read/Write) wait state and EEPROM and Spare (Read) wait states to be configured via bits 8 to 11. EEPROM and SPARE read accesses consist of 2–5 wait states whilst MCLK is High, increasing the read access time, followed by 1 trailing wait state whilst MCLK is Low to allow for a greater bus release time. The Chip revision number appears on bits 12 to 15 when read.

Bit	9	8	ROM (Read/Write) Wait States
	0	0	1
	0	1	2
	1	0	3[1]
	1	1	Unused (3)
Bit	**10**	**11**	**EEPROM ans Spare (Read) Wait States**
	0	0	2+1
	0	1	3+1
	1	0	4+1
	1	1	5+1[1]

Table 18: WAIT_STATE register settings.

Note 1 . The conditions after a reset are:–
ROM wait states= 3, EEPROM and Spare wait states = 5+1.

SYSTEM_CONFIG
(Write / Read Address)

This is a Read/Write register (8 bits wide), which allows the Watchdog Function to be enabled and disabled via bit 9. Note that following a System reset this bit is set Low, thus enabling the watchdog.

Bit	9	Watchdog Function
	0	Enabled
	1	Disabled

Table 19: enableing the Watchdog function through the SYSTEM_CONFIG register

Bits 15 to 10 and 8 are not used and could be set High or Low. The Chip revision number appears on bits 12 to 15 when read.

SYSTEM_ERROR_STATUS

This is an 8 bit wide Read only register, and allows the source of a system reset to be determined via bits 11 to 8. It is reset to all Low after being read. The Chip revision number appears on bits 12 to 15 when read.

Bit 8 : Set during a system reset , when the source of the reset is a PLL_LOCK failure.
Bit 9 : Set during a system reset, when the source of the reset is the Watchdog.
Bit 10 : Set during a system reset, when the source of the reset is a POWER_GOOD failure.
Bit 11 : Set during a system reset, when the source of the reset is the external NRESET_IP. Note that this reset source is only available in Standard Interface Mode.

CHIP_REVISION
(Read Addresses)

The CHIP_REVISION register is a read only register which exists as the high 4 data bits of the Wait State, System Configuration and System Error Status registers. A read of any of these three registers will output the CHIP_REVISION information on bits 15 to 12. This register is intended to allow software discrimination of revisions of the GP2021, both pre production revisions and possible customer specific variants. The initial production version of the GP2021 will have a CHIP_REVISION of 0011.

DATA_RETENT
(Write / Read Address)

This is a byte wide Read/Write register which can be used to store a predetermined value, which can be interrogated in order to determine whether a total power loss (below the data retention level) has occurred.

General Control

IO_CONFIG
(Write / Read Address)

The IO_CONFIG register is a full 16 bit wide read/write register containing two separate elements: A 16 bit wide read location which allows the controlling microprocessor to view the input level on all the Discrete and Multi Function inputs, and a 16 bit wide write location for configuration of the Discreteand Multi Function I/O pins.

IO_CONFIG Read: A read of the IO_CONFIG address will latch the logic level of a number of input pins and output these levels to the microprocessor via the 16 bit data bus. This allows the microprocessor to read the input levels on all the Discrete and Multi Function Inputs from a single location. The bit allocations are as follows:

Bit	Input Pin
15	RXB
14	RXA
13	DISCOP
12	DISCIP
11	MAG1
10	SIGN1
9	MAG0
8	SIGN0
7	MULTI_FN_IO
6	NBRAM
5	DISCIO
4	NARMSYS
3	NBW/WRPROG
2	NMREQ
1	NOPC/NINTELMOT
0	NRW

It should be noted that the usefulness of a number of these inputs as Discrete Inputs for System Control is dependant upon the Interface Mode of the GP2021. For instance it is possible to use the NOPC/NINTELMOT pin as a Discrete Input in ARM System mode if the DEBUG function is disabled, whereas this pin could not be used as a Discrete Input in Standard Interface Mode. Similarly, NMREQ could be used as a Discrete Input in Standard Interface Mode but not in ARM System Mode.

IO_CONFIG Write: The IO_CONFIG write location allows the configuration of the multi purpose I/O pins DISCIO and MULTI_FN_IO. The register bit assignments are as follows:

Bit	Bit Name
15 to 13	Not Used
12	MULTI_FN_IO_SELECT_TIMEMARK
11	MULTI_FN_IO_SELECT_100KHZ
10	MULTI_FN_IO_LEVEL
9 to 8	MULTI_FN_IO_CONFIG
7 to 4	Not Used
3	DISCIO_SELECT_TIMEMARK
2	DISCIO_SELECT_100KHZ
1	DISCIO_LEVEL
0	DISCIO_CONFIG

DISCIO_CONFIG: When set High this bit configures the DISCIO pin as a Discrete Output, when low the DISCIO pin is configured as a Discrete Input. A Master Reset sets the DISCIO_CONFIG bit Low.

DISCIO_SELECT TIMEMARK,
DISCIO_SELECT_100KHZ,
DISCIO_LEVEL:

When configured as an output, the DISCIO pin can be setup to give a signal as determined by Table 20.

Bit			DISCIO output value
3	**2**	**1**	
0	0	0	0
0	0	1	1
0	1	X	100kHz square wave
0	X	X	TIMEMARK

Table 20: DISCIO output selection.

At power on reset, the DISCIO output value = 0 setting is chosen. The 100kHz square wave is derived from the Master Clock and is useful for measuring its drift.

MULTI_FN_IO_SELECT TIMEMARK,
MULTI_FN_IO_SELECT_100KHz,
MULTI_FN_IO_LEVEL:

When configured as an output, the MULTI_FN_IO pin can be setup to give a signal as shown in Table 21

Bit			DISCIO output value
12	**11**	**10**	
0	0	0	0
0	0	1	1
0	1	X	100kHz square wave
0	X	X	TIMEMARK

Table 21: MULTI_FN_IO output selection.

MULTI_FN_IO_CONFIG: These 2 bits configure the function of the MULTI_FN_IO input as follows:

Bits <9:8>	MULTI_FN_IO Function
00	Digital System Test Enable Input
01	TRIGGER Input
10	Discrete Input (See Description) / Scan Clocks Input
11	Discrete Output

Master Reset sets bits 9 and 8 to Low.

MULTI_FN_IO as Digital System Test Enable Input: Allows testing of the Digital Section of the System Board. In this mode, when MULTI_FN_IO is High, the RXA pin replaces the Differential Master Clock Inputs and the RXB pin acts as an RTC Reset input. The PLL_LOCK Filter is also disabled. For more information see the Digital System Test Mode description.

MULTI_FN_IO as TRIGGER Input: The DEBUG function is enabled if in ARM System mode and the MULTI_FN_IO pin acts as the TRIGGER input to the DEBUG block. For more information see the DEBUG Block Description.

MULTI_FN_IO as Discrete Input / Scan Clocks: In this mode the pin has 2 functions: As a discrete input and as the Scan Clocks Input for chip scan path testing. It should be noted that the MULTI_FN_IO pin should only be used as a discrete input with caution. Since the Master Reset default is for MULTI_FN_IO to act as the Digital System Test Enable input it must be guaranteed that anything driving this pin as a discrete input must have a Low output until the IO_CONFIG register can be written to and Discrete Input Mode enabled.

TEST_CONFIG (Write Address)

The TEST_CONFIG register is a 3 bit wide write–only register which complements the TEST_CONTROL register of the Correlator but contains chip test control bits for Peripheral Functions. The register bit assignments are as follows:

Bit	**Bit Name**
10	RTC_TEST_COUNT
9	RTC_RESET_ENABLE
8	WDOG_RESET_DISABLE

RTC_TEST_COUNT : When set High this bit splits up the 24 bit counter of the RTC which counts seconds into a number of 4 bit counters to allow easier chip testing. The 24 bit RTC Counter is not Scan Path Testable. A Master Reset sets the RTC_TEST_COUNT bit Low.

RTC_RESET_ENABLE: When set High this bit enables the RXB pin to act as an RTC Reset input, which then resets the RTC and Watchdog counters whenever RXB is taken high. This function is intended for factory testing of the GP2021. A Master Reset forces the RTC_RESET_ENABLE bit Low.

WDOG_RESET_DISABLE: When set High this bit inhibits the production of System Resets from the Watchdog counter, without disabling the Watchdog Counter itself. This function is intended for Scan Path Testing of the Watchdog and RTC Counters. A Master Reset forces the WDOG_RESET_DISABLE bit Low.

DATA_BUS_TEST (Write / Read Address)

This is a 16 bit read/write register, whose function is to allow a simple test of the 16 bit wide data bus to be performed, by writing a 16 bit number and by checking that the same value can be read back.

ABSOLUTE MAXIMUM RATINGS

These are not the operating conditions, but are the absolute limits which if exceeded, even momentarily, may cause permanent damage.
To ensure sustained correct operation the device should be used within the limits given under Electrical Characteristics.
It is essential for bothV DD and V SS to be present before input signals are applied.

Supply Voltage (V DD) from ground (V SS):	–0.3 to+6.0V
Input Voltage (any input pin):	V_{SS} –0.3V to V_{DD} + 0.3V
Output Voltage (any output pin):	V_{SS} –0.3V to V_{DD} +0.3V
Storage Temperature:	–55°C to +150°C

Electrostatic Discharge Protection (ESD)

The device is able to withstand an electrostatic discharge level of 2kV from 100pF through 1500 between any two pins in either polarity (MIL. Std. 883 Human body model).

Crystal Specification

Frequency:	32.768kHz
Temperature range:	–40ϒC to +85ϒC
Series resistance:	50kΩ typ, 100Ω max
Load capacitance:	10pF typical

ELECTRICAL CHARACTERISTICS

T amb = –40°C to 85 °C, V DD = 5V 10%. The input thresholds and output voltage limits for the logic signal pins are tested and guaranteed by production test. All other parameters are guaranteed by characterisation and design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply Current	I DD		22		mA	0 Channels enabled.
			27		mA	4 Channels enabled.
			32		mA	8 Channels enabled.
			38		mA	12 Channels enabled.
			20	150	µA	Power Down Mode 2.2V – 3.3V (Note 3)
			50	500	µA	Power Down Mode 5.0V (Note 3)
Battery backup Voltage	V BATT	2.2			V	Power Down Mode
All TTL Inputs, with and without Pull–up or Pull–down Resistors: type TTL						
High level Input Voltage		2.0			V	
Low level Input Voltage		0.8			V	
Schmitt Trigger inputs Type ST1						
Positive–going Threshold	VI +		1.9	2.3	V	V DD = 3V
Negative–going Threshold	VI –	0.8	1.2		V	V DD = 3V
Hysteresis	Vh	0.35	0.7		V	V DD = 3V
Schmitt Trigger inputs Type ST2						
Positive–going Threshold	VI +		1.72	2.32	V	
Negative–going Threshold	VI –	0.72	1.10		V	
Hysteresis	Vh	0.3	0.62		V	
Master clocks : type Diff						Note 2
Input Voltage High		0.8V DD			V	D.C. coupled
Input Voltage Low				0.2V DD	V	D.C. coupled
OR						
D.C. coupled differential sinewave (pk–pk)		130			mV	Mid point at nominal 4.3V
OR						
Peak to Peak single sinewave		600			mV	AC coupled
Crystal Oscillator Type XTLI, XTLO						
Frequency Range	f osc		32	1000	kHz	
Amplifier Transconductance	gm	220	550	2500	µA/V	
Output Impedance	Z0	20	56	100	kW	

ELECTRICAL CHARACTERISTICS(cont.)

T amb = –40°C to 85 °C, V DD = 5V 10%. The input thresholds and output voltage limits for the logic signal pins are tested and guaranteed by production test. All other parameters are guaranteed by characterisation and design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Power level 6 Outputs: types OP6 and OPT6						
Output Voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = –12mA
Output Voltage Low	V OL			0.4	V	I_{OL} = 12mA
Output short	IOS		270		mA	V_{DD} = max VO = V DD
circuit current			150		mA	V_{DD} = max VO = 0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V DD
Output capacitance	COUT		5		pF	
Power Level 3 Outputs : types OP3 and OPT3						
Output Voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = –6mA
Output voltage Low	V_{OL}			0.4	V	I_{OL} = 6mA
Output short	IOS		135		mA	V_{DD} = max VO = V_{DD}
circuit current			75		mA	V_{DD} = max VO = 0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	
Power Level 2 Outputs: types OP2 and OPT2						
Output voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = –4mA
Output voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA
Output short	IOS		90		mA	V_{DD} = max VO = V_{DD}
circuit current			50		mA	V_{DD} = max VO =0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	
Power Level 1 Outputs: types OP1 and OPT1						
Output Voltage High	V_{OH}	0.8V DD		V		I_{OH} = –2mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 2mA
Output short	IOS		45		mA	V_{DD} = max VO = V_{DD}
circuit current			25		mA	V_{DD} = mx VO = V_{DD}
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	

Note 1: Any unused inputs must be tied High or Low.

Note 2: The input pair CLK_T, CLK_I may be driven by CMOS logic levels (D.C. coupled) or A.C. coupled or by a low amplitude differential sinewave (D.C. coupled e.g. GP2010). If a single logic level is to be used this should drive CLK_T with the CLK_I pin biased to mid supply. If a single sinewave clock is to be used this should drive CLK_T through a capacitor, with both of the CLK_T/CLK_I pins biased to approximately two thirds supply. See Fig. 24 for a suggested circuit.

Note 3: These values apply when the 32kHz oscillator circuit is not running.

Note 4: The operation of the feature whereby input levels and output drive strengths can be modified is not guaranteed by the existing factory testing procedure.

PIN TYPES

The following Table defines the type of each pin and additional notes relating to them.

Pin No	Pin Name	Pin Type	Input Type	Pull Up/Dn	O/P Type	Tri–State	Notes
1	MULTI_FN_IO	I/O	ST2	75k dn	OPT3	YES	1
2	POWER_GOOD	IP	ST2	none	–	–	
3	NRESET_OP	OP	–	–	OP3	NO	
4	NARMSYSIP	ST2	none	–	–		
5	XIN	IP	XTLI	none	–	–	Xtal In
6	XOUT	OP	–	–	XTLO	NO	Xtal Out
7	TXA	OP	–	–	OP6	NO	
8	TXB	OP	–	–	OP6	NO	
9	RXA	IP	ST2	none	–	–	
10	RXB	IP	ST2	none	–	–	
11	NROM / NC	OP	–	–	OPT6	YES	9
12	NEEPROM / NC	OP	–	–	OPT6	YES	8
13	NSPARE_CS / NC	OP	–	–	OPT6	YES	9
14	V DD	V DD	–	–	–	–	
15	V SS	V SS	–	–	–	–	
16	NRAM / NC	OP	–	–	OP6	NO	10
17	NW0 / NCOP	–	–	OP6	NO	11	
18	NW1 / NCOP	–	–	OP6	NO	10	
19	NW2 / NCOP	–	–	OP6	NO	10	
20	NW3 / NCOP	–	–	OP6	NO	10	
21	NRD / NCOP		–	OP6	NO	11	
22	ARM_ALE / NC	OP	–	–	OP6	NO	8
23	DBE / NC	OP	–	–	OP6	NO	8
24	ACCUM_INT	OP	–	–	OPT1/OPT2	YES	2, 6
25	MEAS_INTOP	–	–	OPT1/OPT2	YES	2, 7	
26	NBW / WRPROG	IP	TTL	none	–	–	
27	NMREQ / DISCIP2	IP	TTL	none	–	–	
28	NOPC / NINTELMOT	IP	TTL	none	–	–	
29	NRW / DISCIP3	IP	TTL	none	–	–	
30	MCLK / NC	OP	–	–	OP6	NO	8
31	ABORT / MICRO_CLK	OP	–	–	OP3	NO	
32	DISCIO I/O	ST2	none	OPT3	YES		
33	A22 / READ	IP	TTL/ST2	none	–	–	3
34	V DD	V DD	–	–	–	–	
35	V SS	V SS	–	–	–	–	
36	A21 / NCS IP TTL/ST2		none	–	–	3	
37	A20 / WREN	IP	TTL/ST2	none	–	–	3
38	A9	IP	TTL	none	–	–	
39	A8	IP	TTL	none	–	–	
40	A7	IP	TTL	none	–	–	
41	A6	IP	TTL	none	–	–	
42	A5	IP	TTL	none	–	–	
43	A4	IP	TTL	none	–	–	
44	A3	IP	TTL	none	–	–	

Pin No	Pin Name	Pin Type	Input Type	Pull Up/Dn	O/P Type	Tri–State	Notes
45	A2	IP	TTL	none	–	–	
46	A1 / ALE_IP I	P	TTL/ST2	none	–	–	3
47	A0 / NRESET_IP	IP	TTL/ST2	none	–	–	3
48	D0	I/O	TTL	none	OPT3/OPT6	YES	4, 12
49	D1	I/O	TTL	none	OPT3/OPT6	YES	4, 12
50	D2	I/O	TTL	none	OPT3/OPT6	YES	4, 12
51	D3	I/O	TTL	none	OPT3/OPT6	YES	4, 12
52	D4	I/O	TTL	none	OPT3/OPT6	YES	4, 12
53	D5	I/O	TTL	none	OPT3/OPT6 Y	ES	4, 12
54	D6	I/O	TTL	none	OPT3/OPT6	YES	4, 12
55	V DD	V DD	–	–	–	–	
56	V SS	V SS	–	–	–	–	
57	D7	I/O	TTL	none	OPT3/OPT6	YES	4, 12
58	D8	I/O	TTL	none	OPT3/OPT6	YES	4, 12
59	D9	I/O	TTL	none	OPT3/OPT6	YES	4, 12
60	D10	I/O	TTL	none	OPT3/OPT6	YES	4, 12
61	D11	I/O	TTL	none	OPT3/OPT6	YES	4, 12
62	D12	I/O	TTL	none	OPT3/OPT6	YES	4, 12
63	D13	I/O	TTL	none	OPT3/OPT6	YES	4, 12
64	D14	I/O	TTL	none	OPT3/OPT6	YES	4, 12
65	D15	I/O	TTL	none	OPT3/OPT6	YES	4, 12
66	PLL_LOCK	IP	ST2	none	–	–	
67	V DD	V DD	–	–	–	–	
68	DISCOP	OP	–	–	OPT3	YES	
69	V SS	V SS	–	–	–	–	
70	CLK_T	IP	Diff	none	–	–	
71	CLK_I	IP	Diff	none	–	–	
72	V SS	V SS	–	–	–	–	
73	SAMPCLK	OP	–	–	OP2	No	13
74	V DD	V DD	–	–	–	–	
75	NBRAM / DISCIP4	IP	ST2	none	–	–	
76	SIGN0	IP	ST2/ST1	none	–	–	5, 13
77	MAG0	IP	ST2/ST1	none	–	–	5, 13
78	SIGN1	IP	ST2/ST1	none	–	–	5, 13
79	MAG1	IP	ST2/ST1	none	–	–	5, 13
80	DISCIP1	IP	ST2	none	–	–	

Notes :
1. Although MULTI_FN_IO is capable of being used as a Discrete input, this is not advised since if this pin is driven High at power up, Digital Test Mode will be selected and correct operation will not ensue.
2. Output has power level 1 when OPS_DRIVE_SEL is Low in the SYSTEM_SETUP Register.
   Output has power level 2 when OPS_DRIVE_SEL is High in the SYSTEM_SETUP Register.
3. Input has TTL thresholds in ARM System mode, but has Schmitt Trigger (type ST2) thresholds in Standard Interface mode.
4. Output has power level 3 when OPS_DRIVE_SEL is Low in the SYSTEM_SETUP Register.
   Output has power level 6 when OPS_DRIVE_SEL is High in the SYSTEM_SETUP Register.
5. Input has Schmitt Trigger type ST2 thresholds when IPS_3V_MODE is Low in the SYSTEM_SETUP Register. When High they have ST1 thresholds.
6. Usually connected to NFIQ of the ARM60 Processor.
7. Usually connected to NIRQ of the ARM60 Processor.
8. Characterisation data for this pin is with C L = 10pF.
9. Characterisation data for this pin is with C L = 20pF.
10. Characterisation data for this pin is with C L = 30pF
11. Characterisation data for this pin is with C L = 50pF.
12. Characterisation data for this pin is with C L = 55pF.
13. Setup and Hold times for the GPS data applied on pins SIGN0, MAG0, SIGN1 and MAG1 are with respect to the rising edge of SAMPCLK. Setup time = 15ns, Hold time = –1ns (i.e. data should not change during the period between 15ns and1ns before the rising edge of SAMPCLK; where SAMPCLK is assumed to be un loaded. The SAMPCLK signal will tend to be further delayed by about 0.1ns / pF of load capacitance).

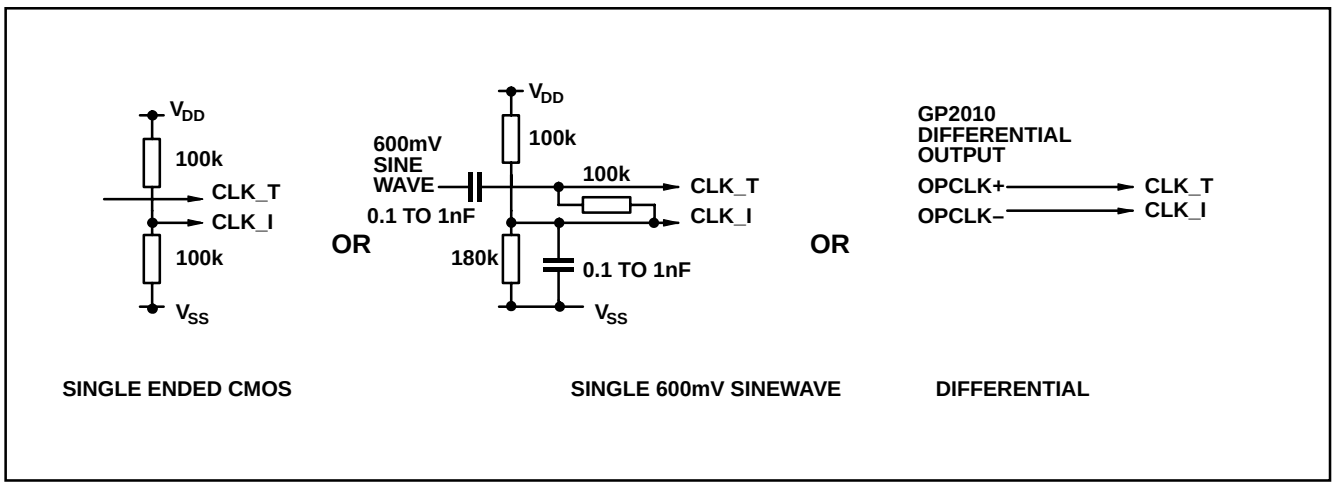


Fig 24 : Clock interconnect options

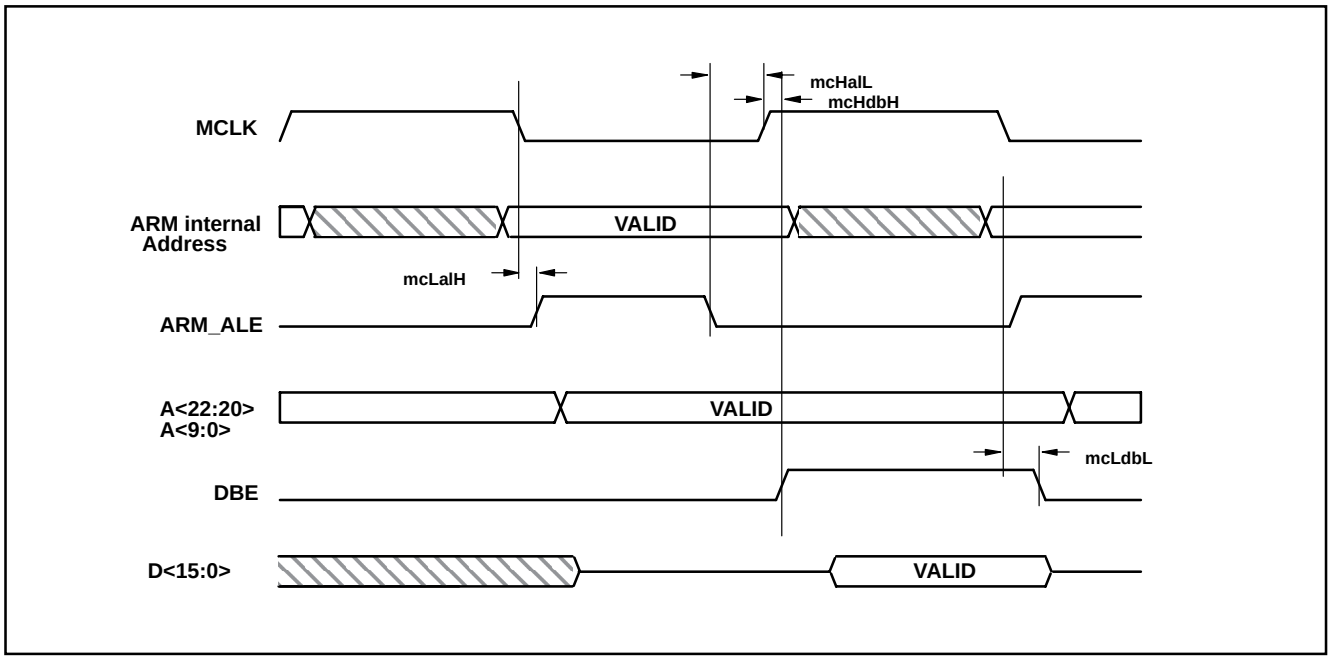


Fig. 25 :GP2021 - ARM60 Interfsce

Description	Symbol	Min	Max	Units
MCLK Low to ALE High	τ_{mcLalH}	–0.5	0	ns
MCLK High to ALE Low	τ_{mcHalL}	0	0.5	ns
MCLK Low to DBE Low	τ_{mcLdbL}	0.5	1.5	ns
MCLK High to DBE High	τ_{mcHdbH}	0.5	1.5	ns

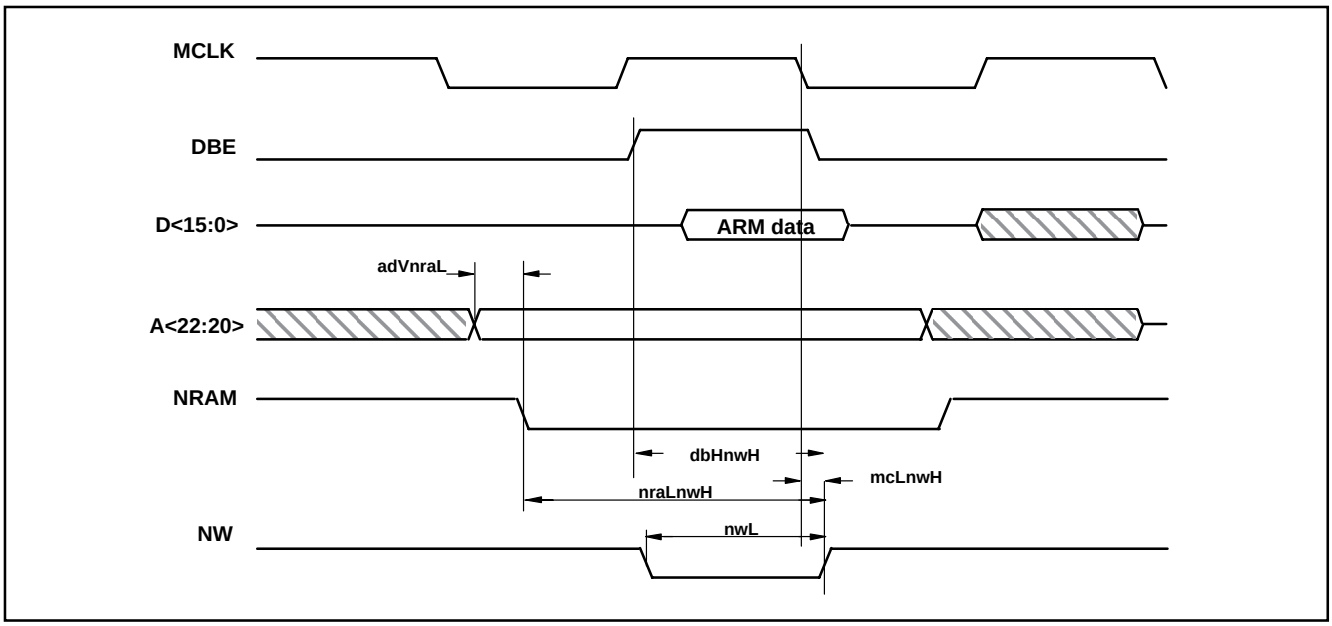


Fig. 26 :ARM Mode RAM Write

Description	Symbol	Min	Max	Units
NRAM Low to NW0–3 High	$\tau_{nraLnwH}$	32	46	ns
MCLK Low to NW0–3 High	τ_{mcLnwH}	0.5	3	ns
DBE High to NW0–3 High	τ_{dbHnwH}	25	27	ns
NW0–3 Low	τ_{nwL}	22	24.5	ns
Address Valid to NRAM Low	$\tau_{adVnraL}$	2	9	ns

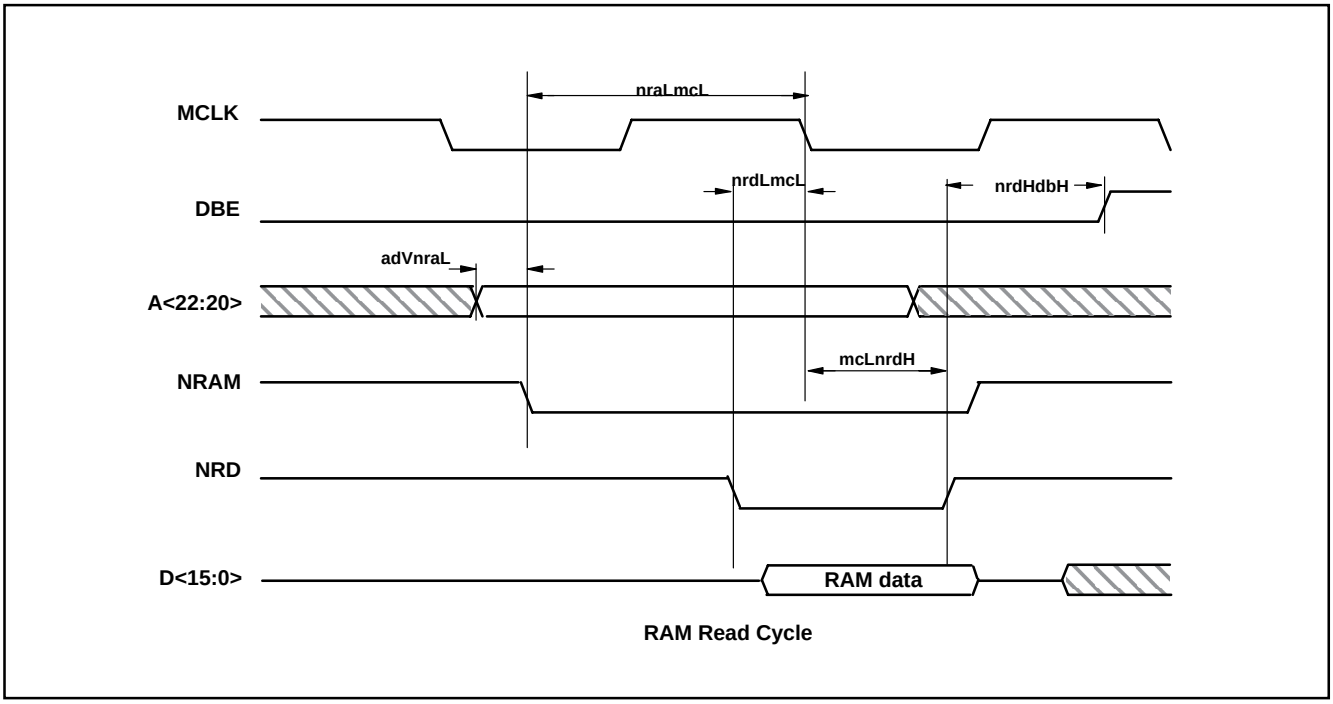


Fig. 27 : ARM Mode RAM Read

Description	Symbol	Min	Max	Units
NRAM Low to MCLK Low	$\tau_{nraLmcL}$	29	45	ns
NRD Low to MCLK Low	$\tau_{nrdLmcL}$	16.5	23	ns
NRD High to DBE High	$\tau_{nrdHdbH}$	15.5	22.5	ns
MCLK Low to NRD High	$\tau_{mcLnrdH}$	2.5	11.5	ns
Address Valid to NRAM Low	$\tau_{adVnraL}$	2	8	ns

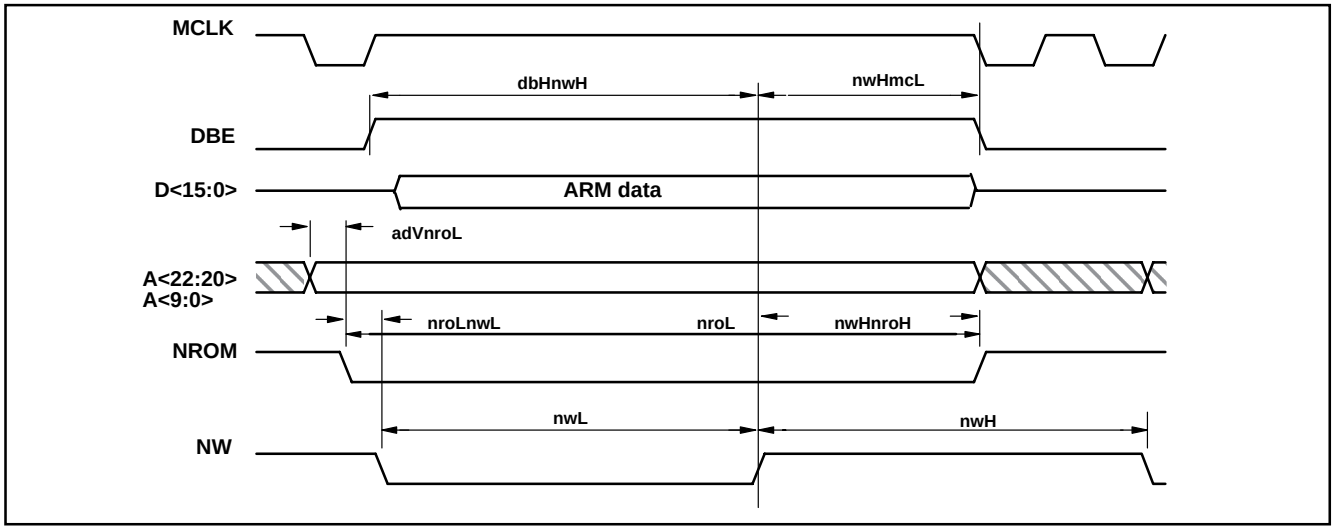


Fig. 27 : ARM Mode RAM Read

Description	Symbol	Min	Max	Units	Notes
NROM Low	τ_{nroL}	100		ns	1
NROM Low to NW0–3 Low	$\tau_{nroLnwL}$	11	21.5	ns	
DBE High to NW0–3 High	τ_{dbHnwH}	52	57	ns	1
NW0–3 Low	τ_{nwL}	50	51	ns	1
NW0–3 High to MCLK Low	τ_{nwHmcL}	16	23	ns	
NW0–3 High to NROM High	$\tau_{nwHnroH}$	27.5	39	ns	
NW0–3 High	τ_{nwH}	47	49	ns	
Address Valid to NROM Low	$\tau_{adVnroL}$	2	7.5	ns	

Note: 1. +50ns / extra wait state

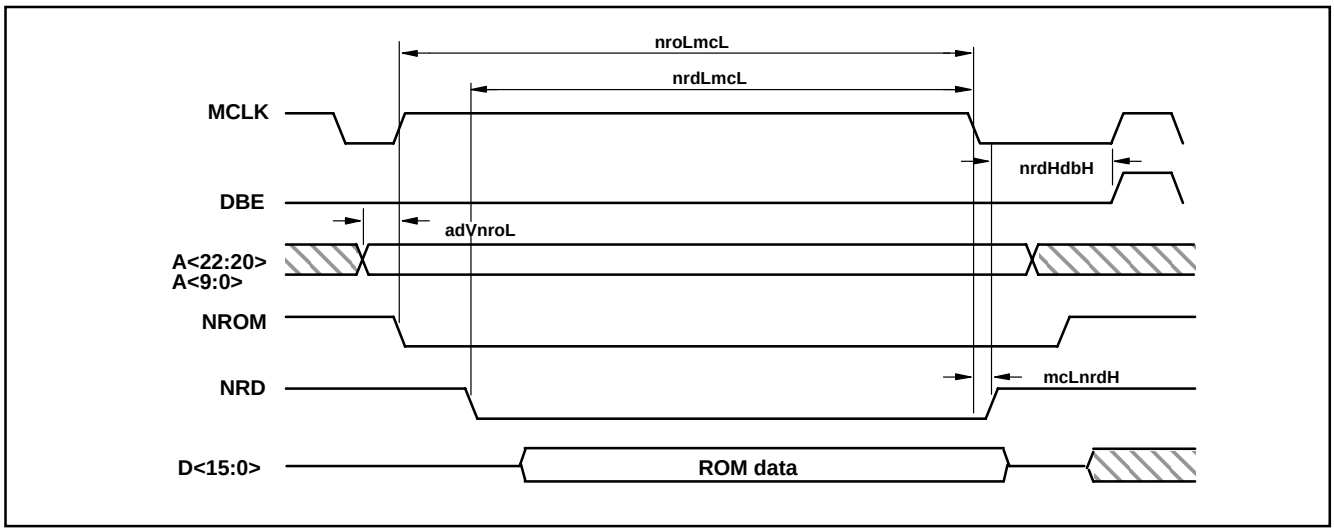


Fig. 27 : ARM Mode ROM Read

Description	Symbol	Min	Max	Units	Notes
NROM Low to MCLK Low	$\tau_{nroLmcL}$	48	74.5	ns	1
NRD Low to MCLK Low	$\tau_{nrdLmcL}$	48	50	ns	1
NRD High to DBE High	$\tau_{nrdHdbH}$	33	45	ns	
MCLK Low to NRD High	$\tau_{mcLnrdH}$	2.5	10	ns	
Address Valid to NROM Low	$\tau_{adVnroL}$	2.5	9	ns	

Note: 1. +50ns / extra wait state

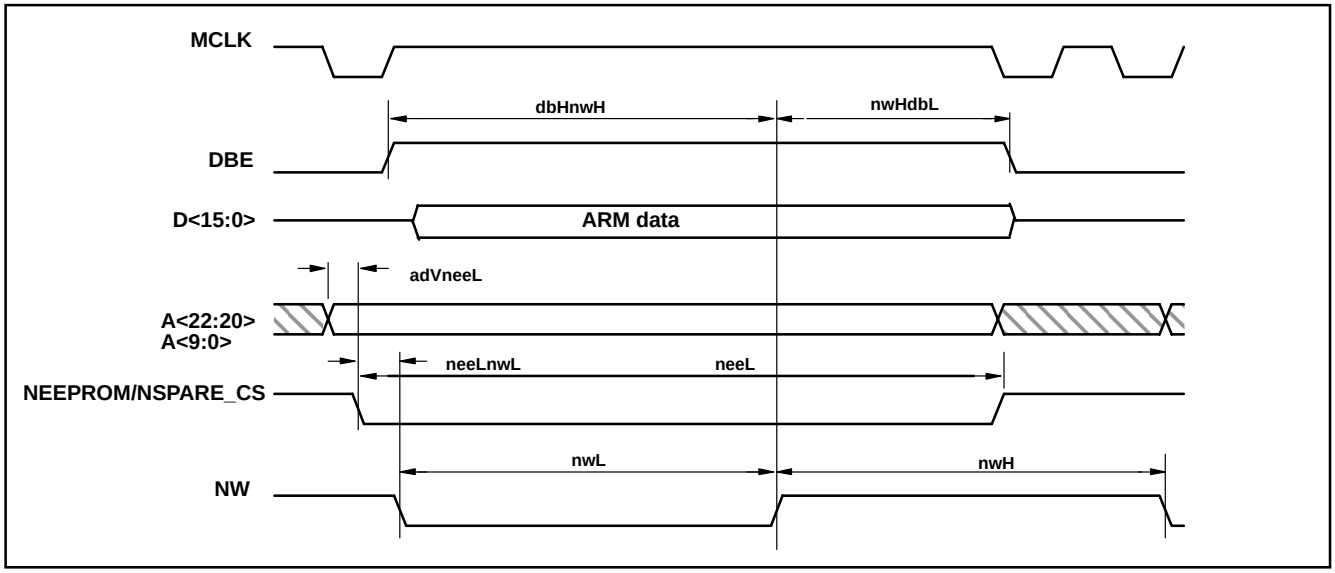


Fig. 27 : ARM Mode RAM Read

Description	Symbol	Min	Max	Units
NEEPROM Low	τ_{neeL}	348		ns
NEEPROM Low to NW0–3	$\tau_{neeLnwL}$	11		ns
NW0–3 Low	$\tau_{nwL\ 1}$	50		ns
NW0–3 High	τ_{nwH}	200		ns
DBE High to NW0–3 High	τ_{dbHnwH}	150		ns
NW0–3 High to DBE Low	τ_{nwHdbL}	168		ns
Address Valid to NEEPROM Low	$\tau_{adVneeL}$	2.5	9	ns

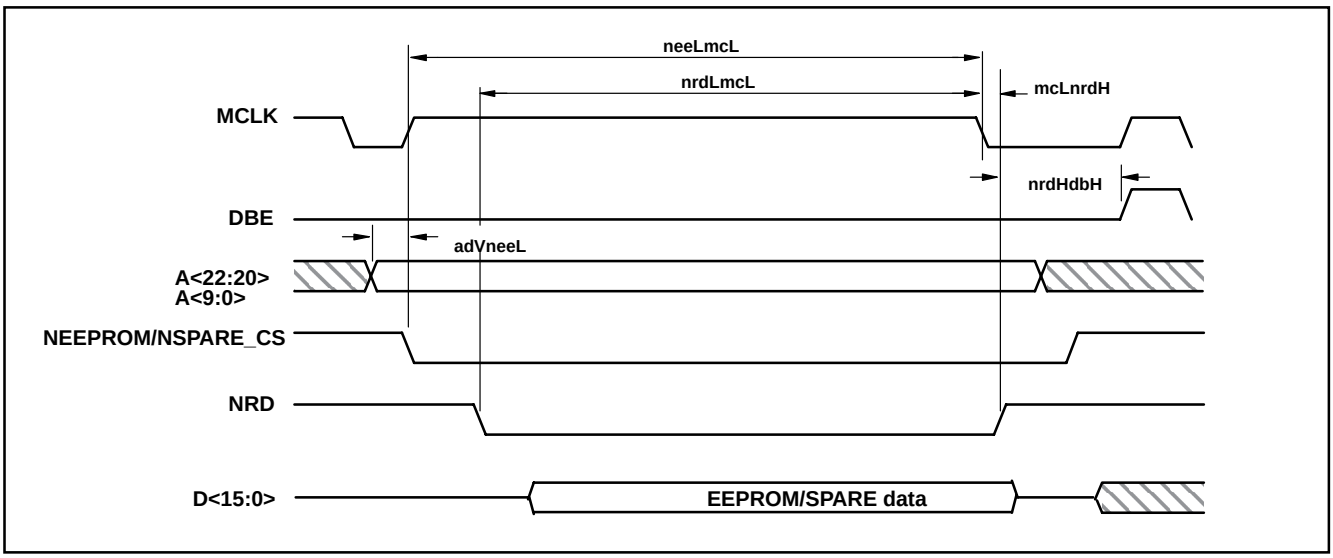


Fig. 27 : ARM Mode RAM Read

Description	Symbol	Min	Max	Units	Notes
NEEPROM Low to MCLK Low	$\tau_{neeLmc}L$	124.5		ns	1
NRD Low to MCLK Low	$\tau_{nrdLmcL}$	117		ns	1
NRD High to DBE High	$\tau_{nrdHdbH}$	65		ns	
MCLK Low to NRD High	$\tau_{mcLnrdH}$	2.5	10	ns	
Address Valid to NEEPROM Low	$\tau_{adVneeL}$	2.5	9	ns	

Note: 1. +50ns / extra wait state

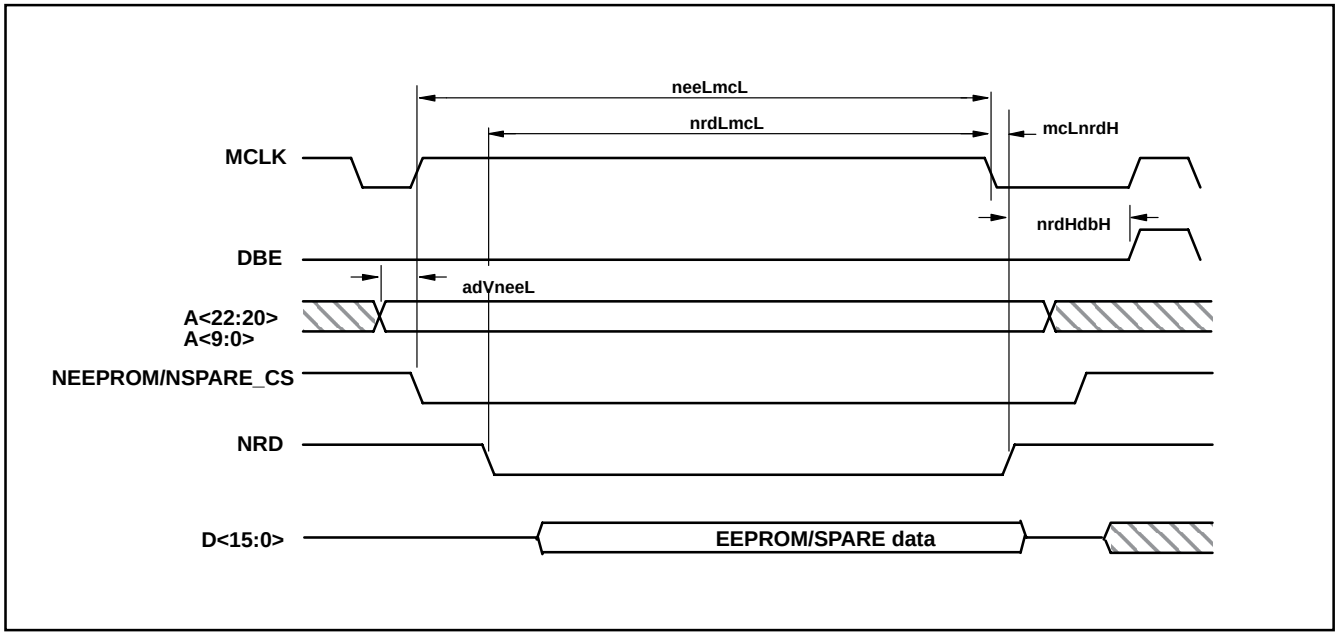


Fig. 32 : Intel 486 mode write (NARMSYS = 1, NINTELMOT = 0, WRPROG = !)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to WREN and NCS Low setup time	τ_{alHwcL}	5		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
ALE_IP Low to WREN or NCS High pulse width	τ_{alLwcH}	10		ns	1
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
WREN or NCS High to ALE_IP High hold–off time	τ_{wcHalH}	5		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

Note: 1 Write inhibited until ALE_IP falling edge.

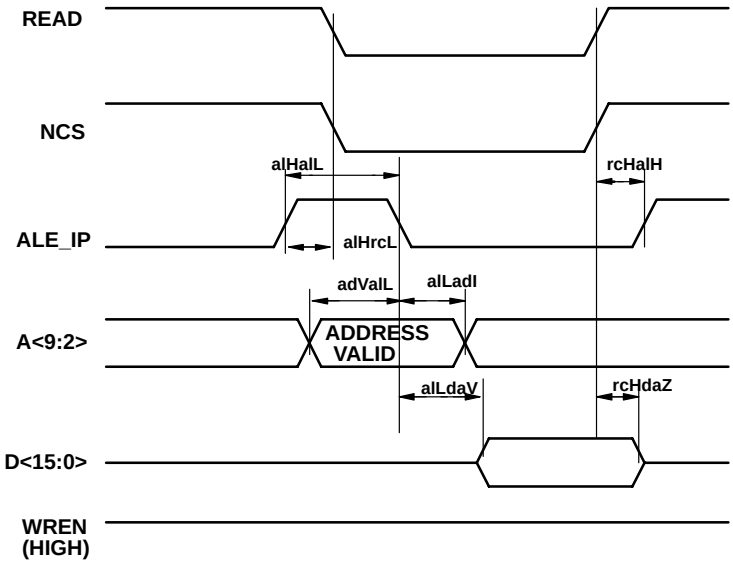


Fig. 33 : Intel 486 mode read (NARMSYS = 1, NINTELMOT = 0, WRPROG = 1)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to WREN and NCS Low setup time	τ_{alHwcL}	5		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
ALE_IP Low to WREN or NCS High pulse width	τ_{alLwcH}	10		ns	1
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
WREN or NCS High to ALE_IP High hold–off time	τ_{wcHalH}	5		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

Note: 1 Write inhibited until ALE_IP falling edge.

2 The ALE_IP Low to Data Output Valid Delay assumes ALE_IP is overlapping the READ and NCS Low time. If not, the τ_{alLda}V parameter applies from the point at which both READ and NCS are Low.

3. The Data Out Propagation delay is for a data bus load of 50pF.

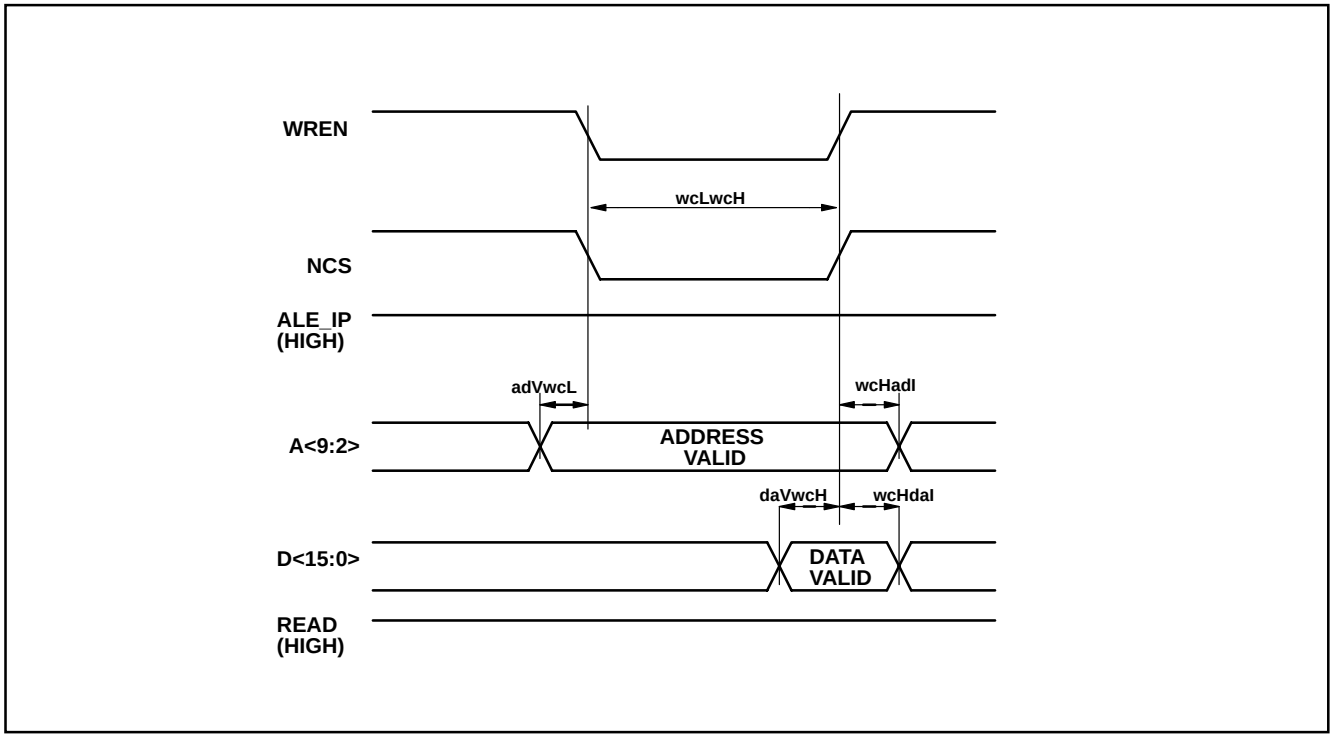


Fig. 34 : Intel 186 mode write with ALE_IP tied High (NARMSYS = 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
Address valid to WREN and NCS Low setup time	τ_{adVwcL}	9		ns	
WREN or NCS High to Address Invalid Hold time	τ_{wcHadI}	10		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

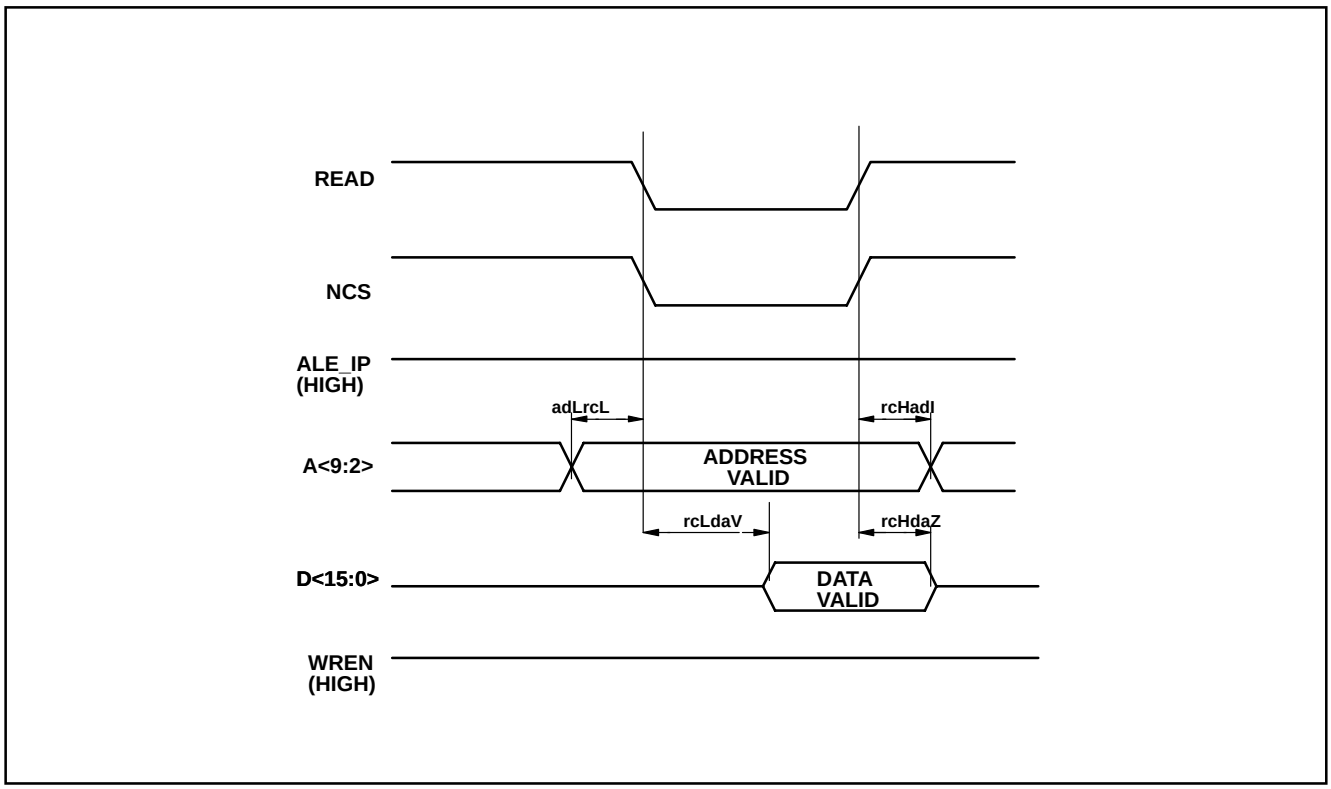


Fig. 35 : Intel 186 mode read with ALE_IP tied High (NARMSYS + 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
Address Valid to READ and NCS Low setup time	τ_{adVrcL}	9		ns	
READ or NCS High to Address Invalid hold time	τ_{rcHadI}	10		ns	
READ and NCS Low to Data Valid propagation delay	τ_{rcLdaV}	44		ns	1
READ or NCS High to Data High Impedance	τ_{rcHdaZ}	4	23	ns	

Notes: 1 The Data Out Propagation delay is for a Data Bus load of 50pF.

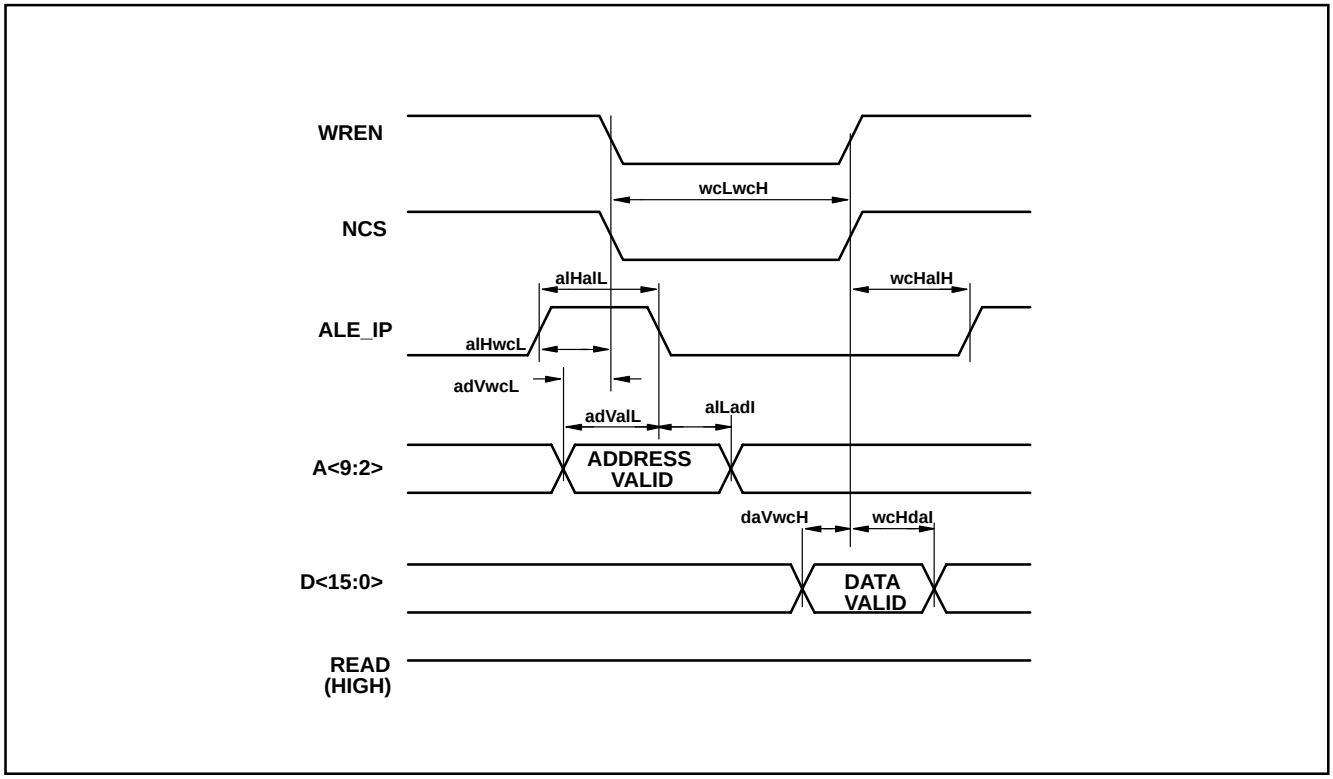


Fig. 36 : Intel 186 mode writewith ALE_IP being pulsed (NARMSYS = 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to WREN and NCS Low setup time	τ_{alHwcL}	14		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	10		ns	
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
WREN or NCS High to ALE_IP High hold off time	τ_{wcHalH}	5		ns	
Address Valid to WREN and NCS Low setup time	τ_{adVwcL}	10		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	8		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

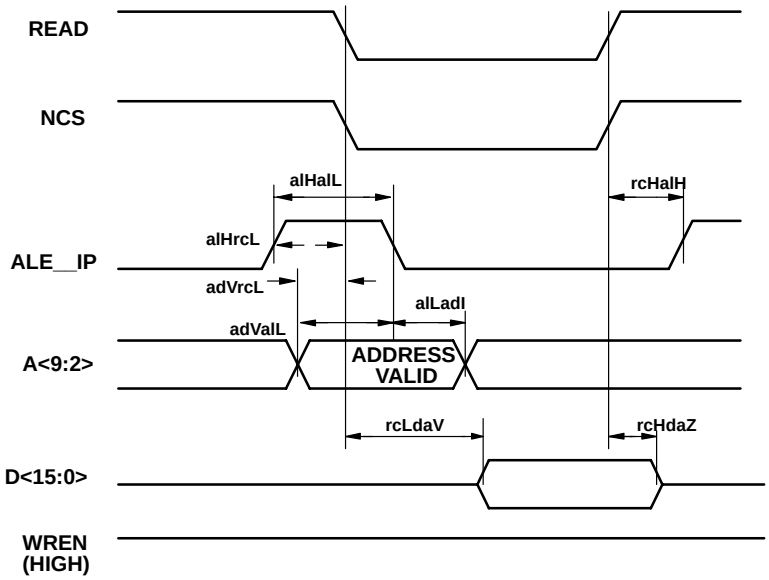


Fig. 37 : Intel 186 mode read ALE_IP being pulsed (NARMSYS = 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to READ and NCS Low setup time	τ_{alHrcL}	14		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	10		ns	
READ or NCS High to ALE_IP High hold off time	τ_{rcHalH}	5		ns	
Address Valid to READ and NCS Low setup time	τ_{adVrcL}	10		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	8		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
READ and NCS Low to Data Valid propagation delay	τ_{rcLdaV}		44	ns	1
READ or NCS High to Data High Impedance	τ_{pcHdaZ}	4	23	ns	

Notes: 1 The Data Out propagation delay is for a Data Bus load of 50pF.

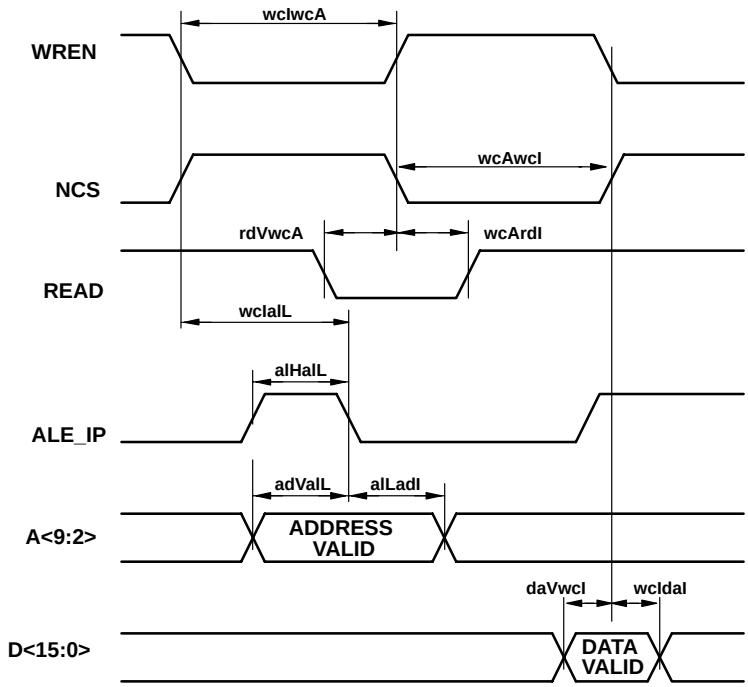


Fig. 38 : Motorola mode write, ALE_IP non-overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
WREN and NCS active to WREN or NCS inactive	τ_{wcAwcl}	10		ns	1
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
WREN or NCS Inactive to ALE_IP Low Hold off time	τ_{wclalL}	23		ns	1
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadl}	8		ns	
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 2
WREN and NCS Active to READ Invalid hold time	τ_{wcArdl}	5		ns	1, 2
DATA Valid to WREN or NCS Inactive setup time	τ_{daVwcl}	7		ns	1
WREN or NCS Inactive to DATA Invalid hold time	τ_{wcldal}	5		ns	1

Notes: 1 WREN is active High, NCS is Active Low.

2 READ is transparently latched by WREN and NCS being active.

3 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the τ_{wclalL} parameter.

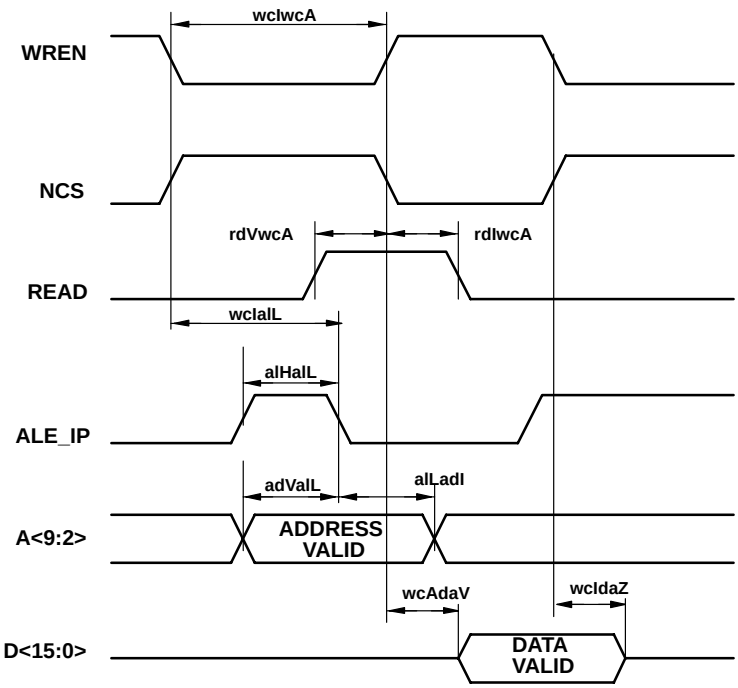


Fig. 39 : Motorola mode read, ALE_IP non-overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
WREN or NCS Inactive to ALE_IP Low Hold off time	τ_{wclalL}	23		ns	1
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid Hold time	τ_{alLadl}	8		ns	
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 2
WREN and NCS Active to READ Invalid Hold time	τ_{wcArdl}	5		ns	1, 2
WREN or NCS Active to DATA valid	τ_{wcAdaV}		44	ns	1
WREN or NCS Inactive to DATA High impedance	τ_{wcldaZ}	4	23	ns	1

Notes: 1 WREN is active High, NCS is active Low.

2 READ is transparently latched by WREN and NCS being active.

3 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the τ_{wclalL} parameter.

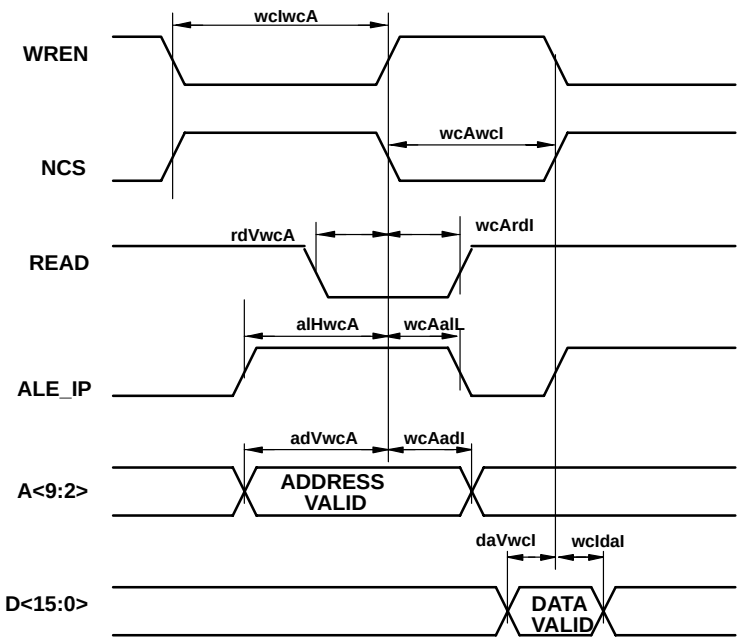


Fig. 40 : Motorola mode read, ALE_IP overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
WREN and NCS Active to WREN or NCS inactive	τ_{wcAwcl}	10		ns	1
ALE_IP High to WREN and NCS Active pulse width	τ_{alHwcA}	13		ns	1
WREN and NCS Active to ALE_IP Low hold time	τ_{wcAalL}	6		ns	1, 2
Address Valid to WREN and NCS Active setup time	τ_{adVwcA}	9		ns	1
WREN and NCS Active to Address Invalid hold time	τ_{wcAadl}	11		ns	1
READ Valid to WREN and NCS Active setup time	τ_{dVwcA}	7		ns	1, 3
WREN and NCS Active to READ Invalid hold time	τ_{wcArdl}	5		ns	1, 3
DATA Valid to WREN or NCS Inactive setup time	τ_{daVwcl}	7		ns	1
WREN or NCS Inactive to DATA Invalid hold time	τ_{wcldal}	5		ns	1

Notes:
1. WREN is active High, NCS is Active Low.
2. If ALE_IP does not overlap WREN and NCS active by wcAalL then the timings for ALE_IP both overlapping and non–overlapping WREN and NCS active must be met.
3. READ is transparently latched by WREN and NCS being active.
4. There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the wclalL parameter.

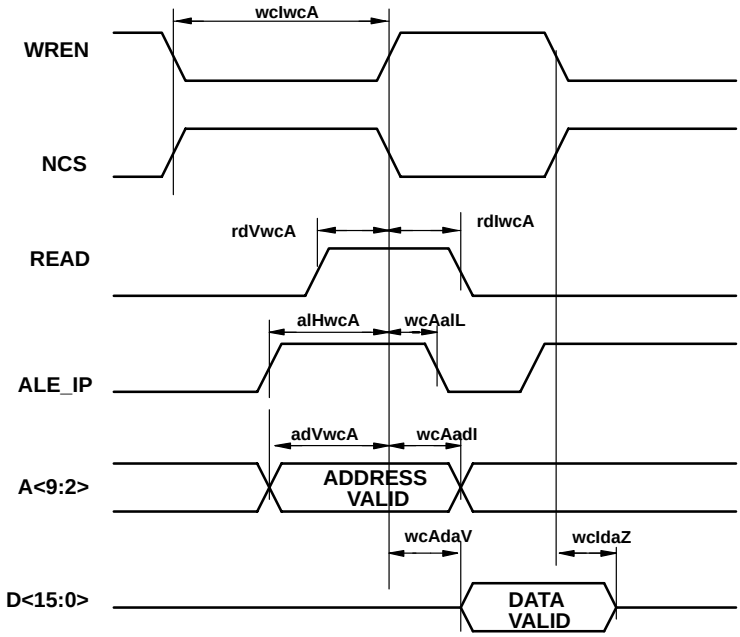


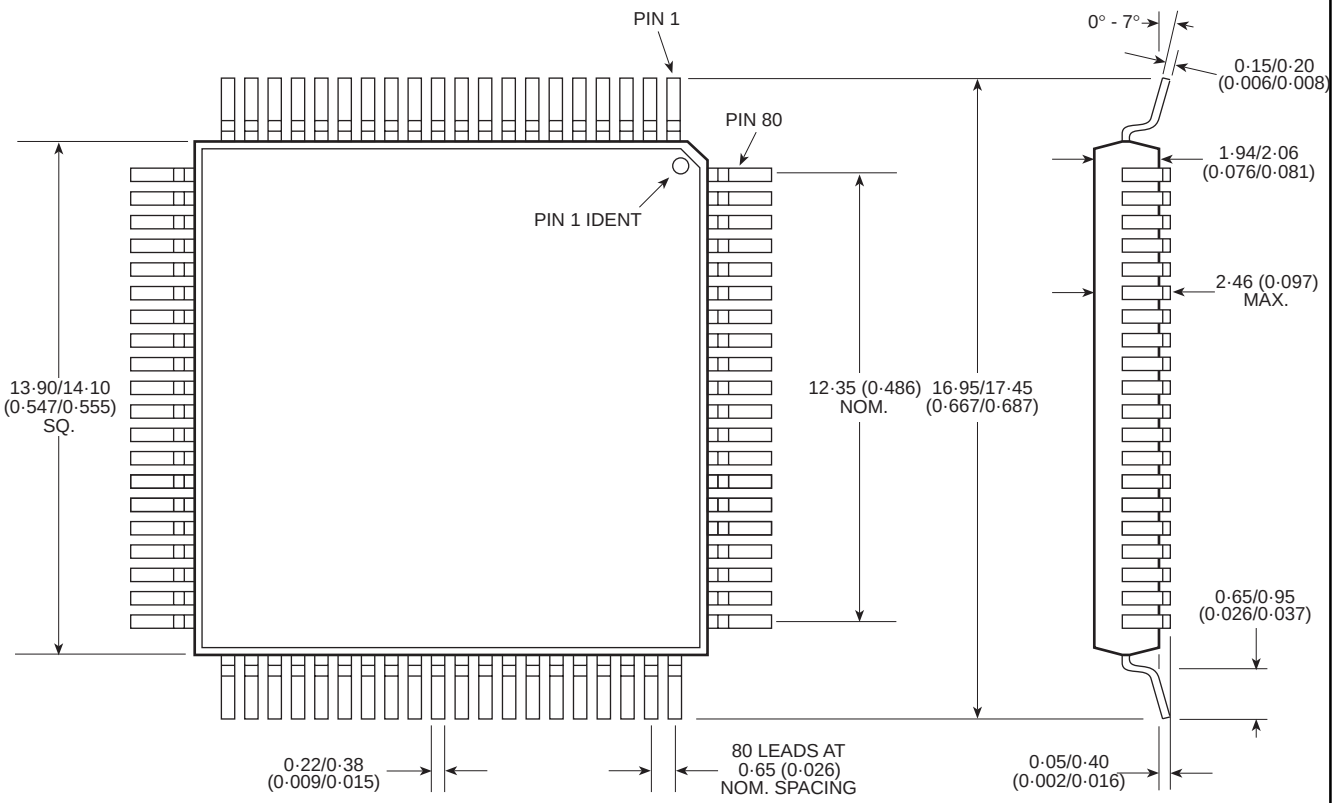
Fig. 41 : Motorola mode read, ALE_IP overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
WREN and NCS Active to WREN or NCS inactive	τ_{wcAwcl}	10		ns	1
ALE_IP High to WREN and NCS Active pulse width	τ_{alHwcA}	13		ns	1
WREN and NCS Active to ALE_IP Low hold time	τ_{wcAalL}	6		ns	1, 2
Address Valid to WREN and NCS Active setup time	τ_{adVwcA}	9		ns	1
WREN and NCS Active to Address Invalid hold time	τ_{wcAadl}	11		ns	1
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 3
WREN and NCS Active to READ Invalid hold time	τ_{wcArdl}	5		ns	1, 3
DATA Valid to WREN or NCS Inactive setup time	τ_{daVwcl}	7		ns	1
WREN or NCS Inactive to DATA Invalid hold time	τ_{wcldal}	5		ns	1

Notes:
1 WREN is active High, NCS is Active Low.
2 If ALE_IP does not overlap WREN and NCS active by wcAalL then the timings for ALE_IP both overlapping and non–overlapping WREN and NCS active must be met.
3 READ is transparently latched by WREN and NCS being active.
4 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the wclalL parameter.

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

80-LEAD PLASTIC QUAD FLATPACK – GQ80

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